

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	LGA1151_A
05	LGA1151_B-DDR4
06	LGA1151_C
07	LGA1151_D
08	DDR4 CHANNEL A 1,2
09	DDR4 CHANNEL B 1,2
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11	PCH DMI,USB,PCIE
12	PCH MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR, GND
15	Dual BIOS
16	ITE 8628 LPC IO
17	HWM
18	FAN CTRL--SIO
19	PCI EXPRESS X16 SLOT
20	PCI EXPRESS X4 SLOT
21	PCI EXPRESS X1 SLOTS
22	PCI EXPRESS X8 SLOT
23	PCI EXPRESS X16 SWITCH
24	M.2(H) X4
25	SATA EXPRESS
26	IR35201 PWM-CPU VCORE
27	IR3553_MOS_1-CPU VCORE
28	IR3553_MOS_2-CPU VCORE
29	VCCPLL
30	RT8120_DDR_CHOKE
31	RT8120_VPP_CHOKE
32	RT8120_PCH-CHOKE
33	DISCRETE POWER
34	NCT3933

SHEET	TITLE
35	IR35201 PWM-VCCGT
36	IR3553_MOS_1-VCCGT
37	IR3570 PWM-VCCSA/IO
38	IR3553-VCCSA
39	IR3553-VCCIO
40	OC BUTTON
41	Creative Sound3Di
42	Audio Amp
43	Audio Power
44	AUDIO Connect
45	DUAL LAN-A~KILLER E2400
46	DUAL LAN-B~I219
47	DUAL USB30_LAN-I219/E2400
48	IDT6V41510_CLK BUFFER
49	COM , LPT , TPM
50	F_PANEL
51	ASM1061
52	HDMI 20 MCDP2800-BA
53	IT8951
54	IT8792
55	D720210 4port Hub-FRONT
56	D720210 4port Hub (Power)
57	DP PORT
58	M.2(D) X4-3
59	M2_SW_3
60	ATX POWER , A_-PROCHOT
61	KB_MS_USB
62	R_USB30
63	F_USB30
64	F_USB20
65	ALPINE RIDGE CIO & DP
66	ALPINE RIDGE POWER
67	TBT TYPE C PORT A
68	U3.1 Type A PORT B

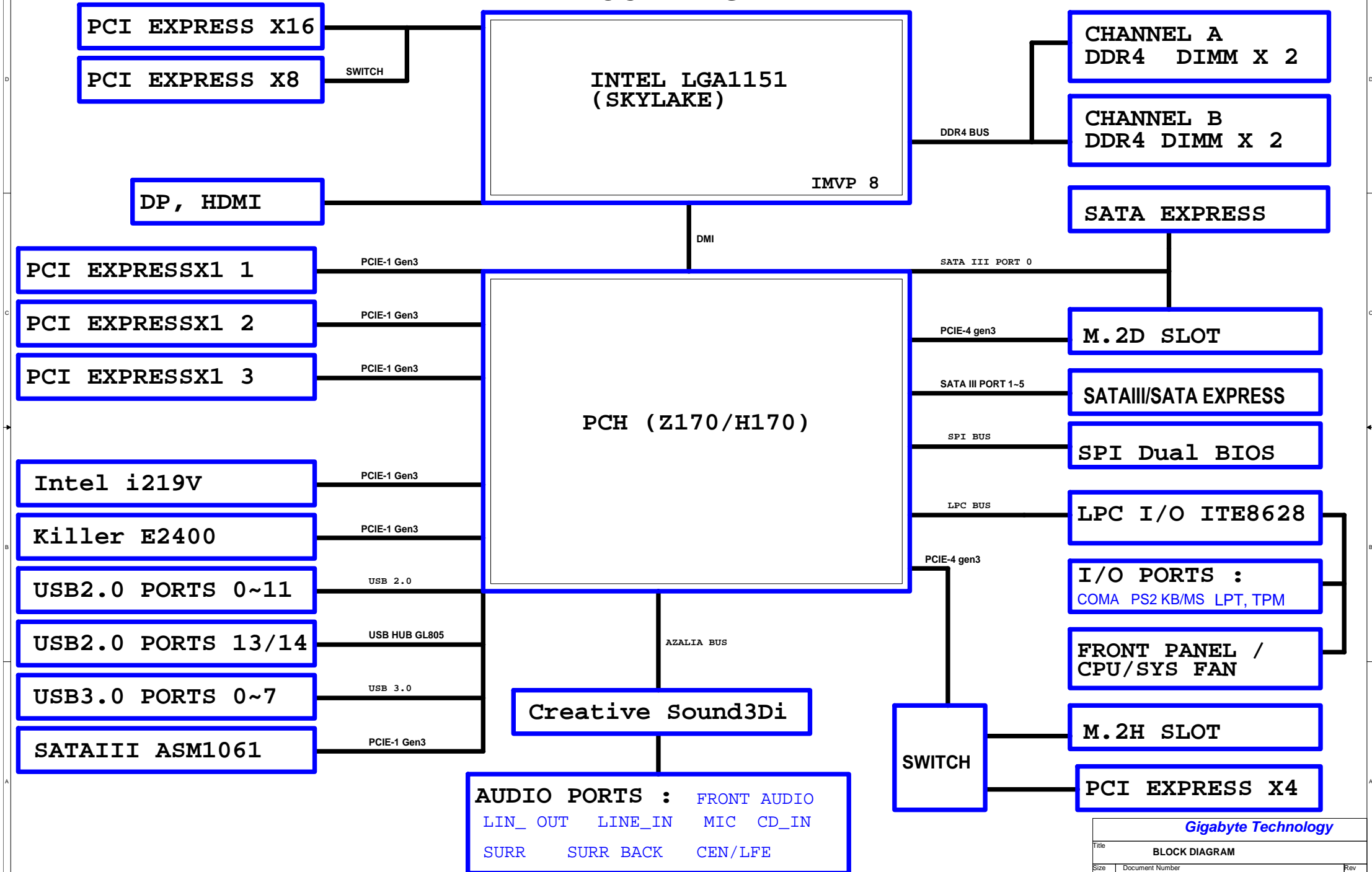
SHEET	TITLE
69	TBT HDMI 2.0
70	BLOCK DIAGRAM
71	EMI-ESD
72	POWER MAP
73	POWER零件使用表
74	TABLE LIST
75	NTC MAP
76	
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Component value change history

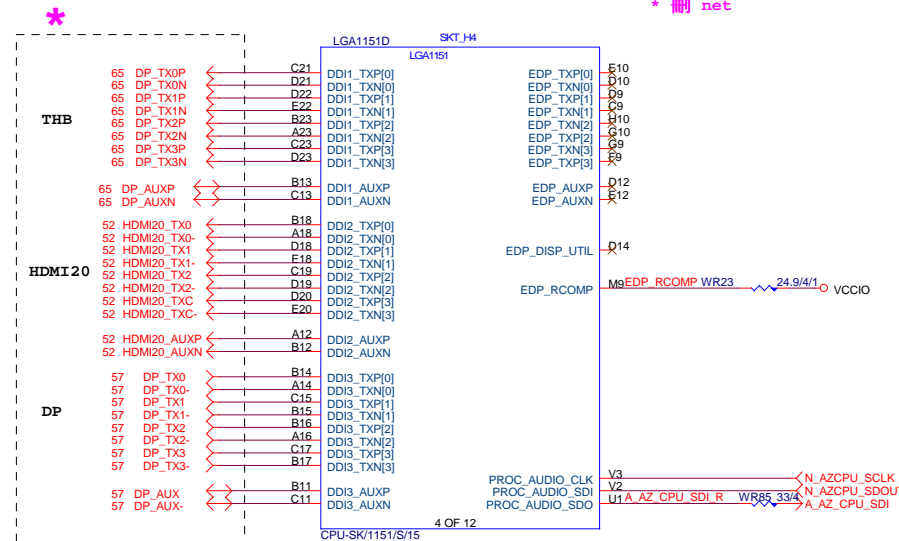
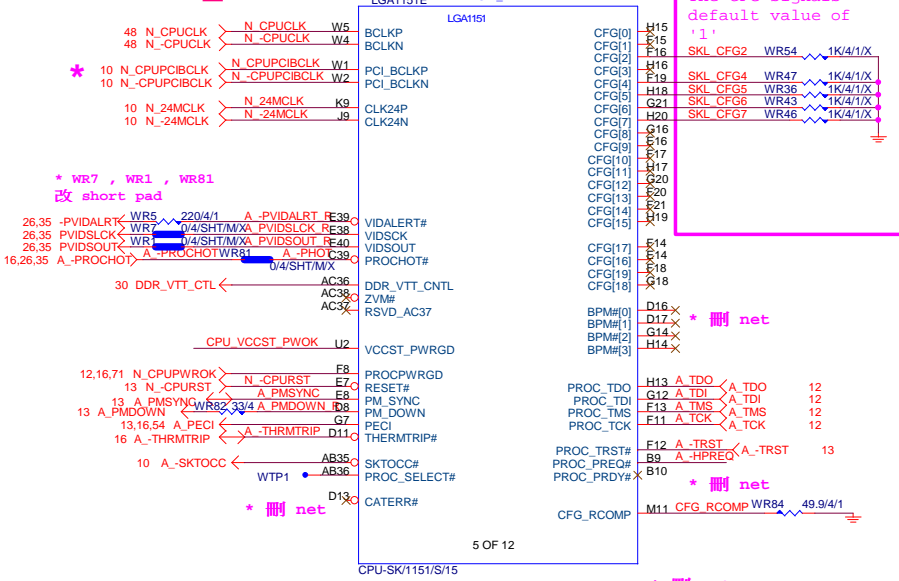
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GIGABYTE™			
Title			
BOM & PCB MODIFY HISTORY			
Size	Document Number		Rev
Custom	GA-Z170X-GAMING GT		1.01
Date:	Wednesday, July 29, 2015	Sheet 2 of	75

BLOCK DIAGRAM

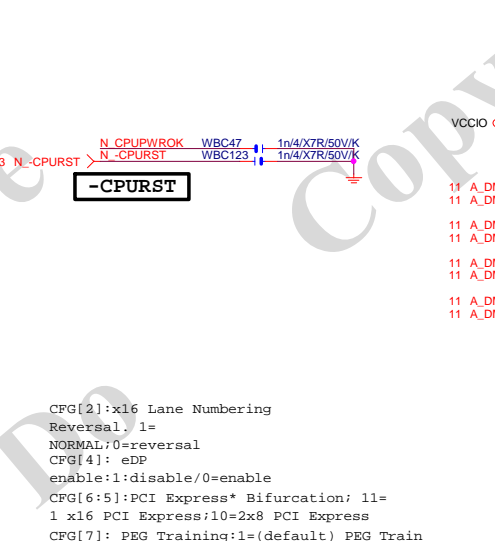
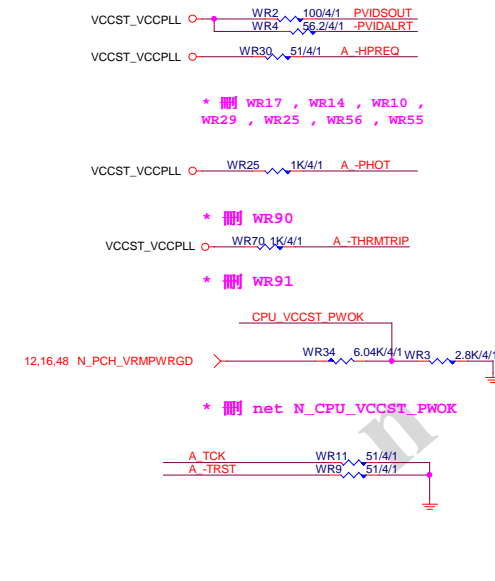


From SKL_0.2B



G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R

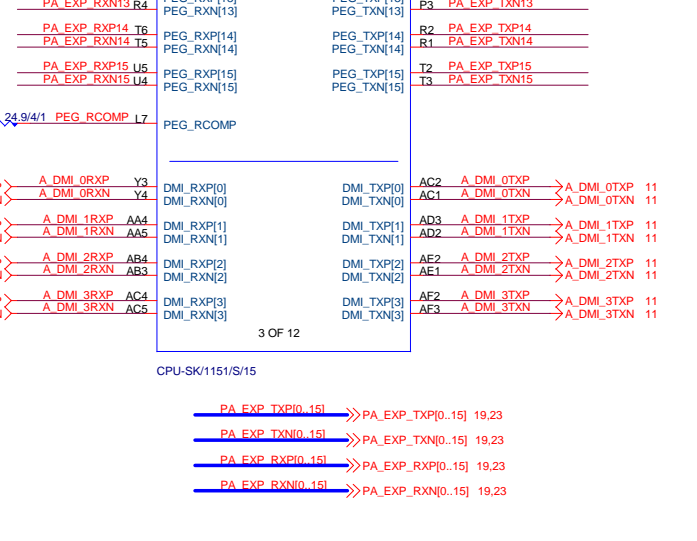
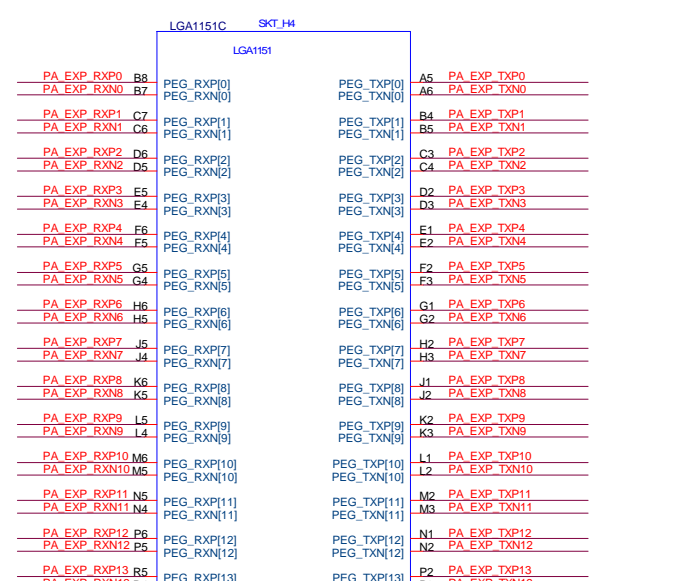
檢查組態調整線路
The CFG signals
default value of
'1'



CFG[2]:x16 Lane Numbering
Reversal, 1=
NORMAL, 0=reversal
CFG[4]: eDP
enable:1:disable/0=enable
CFG[6:5]:PCI Express* Bifurcation: 11=
1 x16 PCI Express:10=2x8 PCI Express
CFG[7]: PEG Training:1=(default) PEG Train
immediately following RESET#;0=PEG Wait
for BIOS

22 -8X_EN < WR37 MASK/0/4/SHT/X SKL_CFG5

Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0



CFG[2]:x16 Lane Numbering
Reversal, 1=
NORMAL, 0=reversal
CFG[4]: eDP
enable:1:disable/0=enable
CFG[6:5]:PCI Express* Bifurcation: 11=
1 x16 PCI Express:10=2x8 PCI Express
CFG[7]: PEG Training:1=(default) PEG Train
immediately following RESET#;0=PEG Wait
for BIOS

22 -8X_EN < WR37 MASK/0/4/SHT/X SKL_CFG5

PA_EXP_TXP[0..15] >>> PA_EXP_TXP[0..15] 19,23
PA_EXP_TXN[0..15] >>> PA_EXP_TXN[0..15] 19,23
PA_EXP_RXP[0..15] >>> PA_EXP_RXP[0..15] 19,23
PA_EXP_RXN[0..15] >>> PA_EXP_RXN[0..15] 19,23

W=12 mil out of CPU
S=15 mil out of CPU

Gigabyte Technology			
CPU LGA1151-A			
Title	Document Number	Rev	1.01
Size	Custom	Rev	1.01
Date:	Thursday, July 23, 2015	Sheet	4 of 75

* 改DDR4 net

LGA1151A SKT_H4

MDA0 AE38	DDR0_DQ[0]	DDR0_CK[0]	AW18 M_DCLKA0	M_DCLKA0 8
MDA1 AE37	DDR0_DQ[1]	DDR0_CK[1]	AV18 M_DCLKA1	M_DCLKA1 8
MDA2 AG38	DDR0_DQ[2]	DDR0_CK[1]	AW17 M_DCLKA1	M_DCLKA1 8
MDA3 AG37	DDR0_DQ[3]	DDR0_CK[1]	AY17 M_DCLKA1	M_DCLKA1 8
MDA4 AE38	DDR0_DQ[4]	DDR0_CK[2]	AW16 M_DCLKA2	M_DCLKA2 8
MDA5 AE40	DDR0_DQ[5]	DDR0_CK[2]	AT16 M_DCLKA2	M_DCLKA2 8
MDA6 AG38	DDR0_DQ[6]	DDR0_CK[3]	AV16 M_DCLKA3	M_DCLKA3 8
MDA7 AG40	DDR0_DQ[7]	DDR0_CK[3]	AY16 M_DCLKA3	M_DCLKA3 8
MDA8 AJ38	DDR0_DQ[8]			
MDA9 AJ37	DDR0_DQ[9]	DDR0_CKE[0]	AY24 CKEA0	CKEA0 8
MDA10 AL38	DDR0_DQ[10]	DDR0_CKE[1]	AV24 CKEA1	CKEA1 8
MDA11 AL37	DDR0_DQ[11]	DDR0_CKE[2]	AV23 CKEA2	CKEA2 8
MDA12 AL40	DDR0_DQ[12]	DDR0_CKE[3]	AV25 CKEA3	CKEA3 8
MDA13 AJ38	DDR0_DQ[13]			
MDA14 AL39	DDR0_DQ[14]	DDR0_CS[0]	AW12 M_CSA0	M_CSA0 8
MDA15 AL40	DDR0_DQ[15]	DDR0_CS[1]	AV12 M_CSA1	M_CSA1 8
MDA16 AJ38	DDR0_DQ[16]	DDR0_CS[2]	AY10 M_CSA2	M_CSA2 8
MDA17 AN40	DDR0_DQ[17]	DDR0_CS[3]	AV10 M_CSA3	M_CSA3 8
MDA18 AR38	DDR0_DQ[18]			
MDA19 AR37	DDR0_DQ[19]	DDR0_ODT[0]	AW11 M_ODT A0	
MDA20 AN39	DDR0_DQ[20]	DDR0_ODT[1]	AV14 M_ODT A1	
MDA21 AN37	DDR0_DQ[21]	DDR0_ODT[2]	AY10 M_ODT A3	
MDA22 AR39	DDR0_DQ[22]	DDR0_ODT[3]		
MDA23 AR40	DDR0_DQ[23]			
MDA24 AW37	DDR0_DQ[24]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AY13 SBAA0	SBAA0 8
MDA25 AL38	DDR0_DQ[25]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AV15 SBAA1	SBAA1 8
MDA26 AV35	DDR0_DQ[26]	DDR0_BA[2]/DDR0_CAB[5]/DDR0_BG[0]	AW23 BG A0	BG A0 8
MDA27 AW36	DDR0_DQ[27]			
MDA28 AJ37	DDR0_DQ[28]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AW13 MAAA16	
MDA29 AV37	DDR0_DQ[29]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AV14 MAAA14	
MDA30 AT36	DDR0_DQ[30]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AY11 MAAA15	
MDA31 AJ38	DDR0_DQ[31]			
MDA32 AY38	DDR0_DQ[32]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AW15 MAAA0	
MDA33 AW38	DDR0_DQ[33]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AV18 MAAA1	
MDA34 AV6	DDR0_DQ[34]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY17 MAAA2	
MDA35 AV6	DDR0_DQ[35]	DDR0_MA[3]	AV19 MAAA3	
MDA36 AV8	DDR0_DQ[36]	DDR0_MA[4]	AT19 MAAA4	
MDA37 AV8	DDR0_DQ[37]	DDR0_MA[5]	AV20 MAAA5	
MDA38 AV8	DDR0_DQ[38]	DDR0_MA[6]	AV21 MAAA6	
MDA39 AV6	DDR0_DQ[39]	DDR0_MA[7]	AT20 MAAA7	
MDA40 AY4	DDR0_DQ[40]	DDR0_MA[8]	AT22 MAAA8	
MDA41 AV4	DDR0_DQ[41]	DDR0_MA[9]	AV22 MAAA11	
MDA42 AT2	DDR0_DQ[42]	DDR0_MA[10]	AV22 MAAA12	
MDA43 AT2	DDR0_DQ[43]	DDR0_MA[11]	AV22 MAAA13	
MDA44 AV3	DDR0_DQ[44]	DDR0_MA[12]	AV23 BG A1	BG A1 8
MDA45 AW4	DDR0_DQ[45]	DDR0_MA[13]	AV24 M_ACT A	M_ACT A 8
MDA46 AT4	DDR0_DQ[46]	DDR0_MA[14]		
MDA47 AT3	DDR0_DQ[47]	DDR0_MA[15]		
MDA48 AP2	DDR0_DQ[48]	DDR0_PAR	AY15	M_DDR_PARA 8
MDA49 AM4	DDR0_DQ[49]	DDR0_ALERT#	AT23	M_ALERT_A 8
MDA50 AP3	DDR0_DQ[50]			
MDA51 AM3	DDR0_DQ[51]			
MDA52 AP4	DDR0_DQ[52]	DDR0_DQS[0]	AF38 M_DQSA0	
MDA53 AM2	DDR0_DQ[53]	DDR0_DQS[1]	AK39 M_DQSA1	
MDA54 AP1	DDR0_DQ[54]	DDR0_DQS[2]	AP39 M_DQSA2	
MDA55 AM1	DDR0_DQ[55]	DDR0_DQS[3]	AW36 M_DQSA3	
MDA56 AK3	DDR0_DQ[56]	DDR0_DQS[4]	AW7 M_DQSA4	
MDA57 AH1	DDR0_DQ[57]	DDR0_DQS[5]	AJ3 M_DQSA5	
MDA58 AK4	DDR0_DQ[58]	DDR0_DQS[6]	AJ3 M_DQSA6	
MDA59 AH2	DDR0_DQ[59]	DDR0_DQS[7]	AN3 M_DQSA7	
MDA60 AH4	DDR0_DQ[60]			
MDA61 AK2	DDR0_DQ[61]	DDR0_DQSP[0]	AF38 M_DQSA0	
MDA62 AH3	DDR0_DQ[62]	DDR0_DQSP[1]	AK38 M_DQSA1	
MDA63 AK1	DDR0_DQ[63]	DDR0_DQSP[2]	AV36 M_DQSA2	
		DDR0_DQSP[3]	AV36 M_DQSA3	
		DDR0_DQSP[4]	AV7 M_DQSA4	
		DDR0_DQSP[5]	AJ2 M_DQSA5	
		DDR0_DQSP[6]	AJ2 M_DQSA6	
		DDR0_DQSP[7]	AN2 M_DQSA7	
		DDR0_DQSP[8]	AV32 M_DQSA8	M_DQSA8 8
		DDR0_DQSP[9]	AV32 M_DQSA8	M_DQSA8 8

8 MDA_ECC[0..7] ↔ MDA_ECC[0..7]

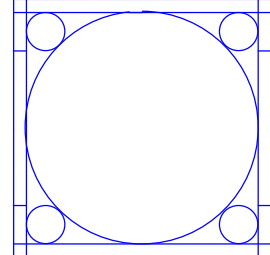
DDR CHANNEL A

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LGA1151

CPU-SK1151/S/15

ILM_BP/1156/CSP/12KRC-0F0001-61R1



Need check the new CPU MB

LGA1151B SKT_H4

MDB0 AD34	DDR1_DQ[0]/DDR0_DQ[16]	DDR1_CK[0]	AM20 M_DCLKB0	M_DCLKB0 9
MDB1 AD35	DDR1_DQ[1]/DDR0_DQ[17]	DDR1_CK[1]	AM21 M_DCLKB1	M_DCLKB1 9
MDB2 AG35	DDR1_DQ[2]/DDR0_DQ[18]	DDR1_CK[2]	AP22 M_DCLKB2	M_DCLKB2 9
MDB3 AH35	DDR1_DQ[3]/DDR0_DQ[19]	DDR1_CK[3]	AP21 M_DCLKB3	M_DCLKB3 9
MDB4 AE35	DDR1_DQ[4]/DDR0_DQ[20]	DDR1_CK[2]	AN20 M_DCLKB2	M_DCLKB2 9
MDB5 AE34	DDR1_DQ[5]/DDR0_DQ[21]	DDR1_CK[1]	AN21 M_DCLKB3	M_DCLKB3 9
MDB6 AG34	DDR1_DQ[6]/DDR0_DQ[22]	DDR1_CK[0]	AP19 M_DCLKB3	M_DCLKB3 9
MDB7 AH34	DDR1_DQ[7]/DDR0_DQ[23]	DDR1_CK[3]	AP20 M_DCLKB3	M_DCLKB3 9
MDB8 AK35	DDR1_DQ[8]/DDR0_DQ[24]			
MDB9 AL35	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CKE[0]	AY29 CKEB0	CKEB0 9
MDB10 AL32	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CKE[1]	AY29 CKEB1	CKEB1 9
MDB11 AL32	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_CKE[2]	AY29 CKEB2	CKEB2 9
MDB12 AK34	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_CKE[3]	AY29 CKEB3	CKEB3 9
MDB13 AL34	DDR1_DQ[13]/DDR0_DQ[29]			
MDB14 AK31	DDR1_DQ[14]/DDR0_DQ[30]	DDR1_CS[0]	AP17 M_CSB0	M_CSB0 9
MDB15 AL31	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_CS[1]	AN15 M_CSB1	M_CSB1 9
MDB16 AP35	DDR1_DQ[16]/DDR0_DQ[32]	DDR1_CS[2]	AM15 M_CSB2	M_CSB2 9
MDB17 AN35	DDR1_DQ[17]/DDR0_DQ[33]	DDR1_CS[3]	AM15 M_CSB3	M_CSB3 9
MDB18 AN32	DDR1_DQ[18]/DDR0_DQ[34]			
MDB19 AP32	DDR1_DQ[19]/DDR0_DQ[35]	DDR1_ODT[0]	AM16 M_ODT B0	
MDB20 AN34	DDR1_DQ[20]/DDR0_DQ[36]	DDR1_ODT[1]	AL16 M_ODT B1	
MDB21 AP34	DDR1_DQ[21]/DDR0_DQ[37]	DDR1_ODT[2]	AL17 M_ODT B2	
MDB22 AN31	DDR1_DQ[22]/DDR0_DQ[38]	DDR1_ODT[3]	AL15 M_ODT B3	
MDB23 AP31	DDR1_DQ[23]/DDR0_DQ[39]			
MDB24 AL29	DDR1_DQ[24]/DDR0_DQ[40]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	AN18 MAA16	
MDB25 AM29	DDR1_DQ[25]/DDR0_DQ[41]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AL17 MAA17	
MDB26 AP29	DDR1_DQ[26]/DDR0_DQ[42]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AP16 MAA15	
MDB27 AR29	DDR1_DQ[27]/DDR0_DQ[43]			
MDB28 AM28	DDR1_DQ[28]/DDR0_DQ[44]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	AL18 SBAB0	SBAB0 9
MDB29 AL28	DDR1_DQ[29]/DDR0_DQ[45]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	AM18 SBAB1	SBAB1 9
MDB30 AR28	DDR1_DQ[30]/DDR0_DQ[46]	DDR1_BA[2]/DDR1_CAB[5]/DDR1_BA[2]	AW28 BG B0	BG B0 9
MDB31 AR28	DDR1_DQ[31]/DDR0_DQ[47]			
MDB32 AR12	DDR1_DQ[32]/DDR0_DQ[48]			
MDB33 AP12	DDR1_DQ[33]/DDR0_DQ[49]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	AL19 MAA19	
MDB34 AM13	DDR1_DQ[34]/DDR0_DQ[50]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	AL22 MAA18	
MDB35 AL13	DDR1_DQ[35]/DDR0_DQ[51]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	AM22 MAA18	
MDB36 AR13	DDR1_DQ[36]/DDR0_DQ[52]	DDR1_MA[3]	AM23 MAA18	
MDB37 AP13	DDR1_DQ[37]/DDR0_DQ[53]	DDR1_MA[4]	AP23 MAA18	
MDB38 AM12	DDR1_DQ[38]/DDR0_DQ[54]	DDR1_MA[5]	AP23 MAA18	
MDB39 AL12	DDR1_DQ[39]/DDR0_DQ[55]	DDR1_MA[6]	AY26 MAA18	
MDB40 AP10	DDR1_DQ[40]/DDR0_DQ[56]	DDR1_MA[7]	AY26 MAA18	
MDB41 AR10	DDR1_DQ[41]/DDR0_DQ[57]	DDR1_MA[8]	AY27 MAA18	
MDB42 AR7	DDR1_DQ[42]/DDR0_DQ[58]	DDR1_MA[9]	AY27 MAA18	
MDB43 AP7	DDR1_DQ[43]/DDR0_DQ[59]	DDR1_MA[10]	AJ27 MAA18	
MDB44 AR9	DDR1_DQ[44]/DDR0_DQ[60]	DDR1_MA[11]	AV27 MAA18	
MDB45 AP9	DDR1_DQ[45]/DDR0_DQ[61]	DDR1_MA[12]	AV27 MAA18	
MDB46 AR6	DDR1_DQ[46]/DDR0_DQ[62]	DDR1_MA[13]	AY28 BG B1	BG B1 9
MDB47 AP6	DDR1_DQ[47]/DDR0_DQ[63]	DDR1_MA[14]	AY28 M_ACT B	M_ACT B 9
MDB48 AM10	DDR1_DQ[48]	DDR1_MA[15]		
MDB49 AL10	DDR1_DQ[49]	DDR1_PAR	AL20	M_DDR_PARB 9
MDB50 AM7	DDR1_DQ[50]	DDR1_ALERT#	AY25	M_ALERT_B 9
MDB51 AL7	DDR1_DQ[51]			
MDB52 AM8	DDR1_DQ[52]			
MDB53 AL9	DDR1_DQ[53]	DDR1_DQS[0]/DDR0_DQS[2]	AF34 M_DQSB0	
MDB54 AM6	DDR1_DQ[54]	DDR1_DQS[1]/DDR0_DQS[3]	AK33 M_DQSB1	
MDB55 AL6	DDR1_DQ[55]	DDR1_DQS[2]/DDR0_DQS[4]	AN33 M_DQSB2	
MDB56 AJ6	DDR1_DQ[56]	DDR1_DQS[3]/DDR0_DQS[5]	AN29 M_DQSB3	
MDB57 AJ7	DDR1_DQ[57]	DDR1_DQS[4]/DDR0_DQS[6]	AN13 M_DQSB4	
MDB58 AF6	DDR1_DQ[58]	DDR1_DQS[5]/DDR0_DQS[7]	AM8 M_DQSB5	
MDB59 AF7	DDR1_DQ[59]	DDR1_DQS[6]/DDR0_DQS[8]	AG6 M_DQSB7	
MDB60 AH7	DDR1_DQ[60]			
MDB61 AH6	DDR1_DQ[61]	DDR1_DQSP[0]	AF35 M_DQSB0	
MDB62 AF7	DDR1_DQ[62]	DDR1_DQSP[1]	AL33 M_DQSB1	
MDB63 AF6	DDR1_DQ[63]	DDR1_DQSP[2]	AN28 M_DQSB2	
		DDR1_DQSP[3]	AN28 M_DQSB3	
		DDR1_DQSP[4]	AN12 M_DQSB4	
		DDR1_DQSP[5]	AP8 M_DQSB5	
		DDR1_DQSP[6]	AL8 M_DQSB6	
		DDR1_DQSP[7]	AG7 M_DQSB7	
		DDR1_DQSP[8]	AN25 M_DQSB8	M_DQSB8 9
		DDR1_DQSP[9]	AN26 M_DQSB8	M_DQSB8 9

9 MDB_ECC[0..7] ↔ MDB_ECC[0..7]

DDR CHANNEL B

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CPU-SK1151/S/15

8 MODT_A[0..3] ↔ MODT_A[0..3]

9 MODT_B[0..3] ↔ MODT_B[0..3]

8 MDA[0..63] ↔ MDA[0..63]

9 MDB[0..63] ↔ MDB[0..63]

8 M_DQSA[0..7] ↔ M_DQSA[0..7]

8 M_DQSA[0..7] ↔ M_DQSA[0..7]

8 MAA[0..16] ↔ MAA[0..16]

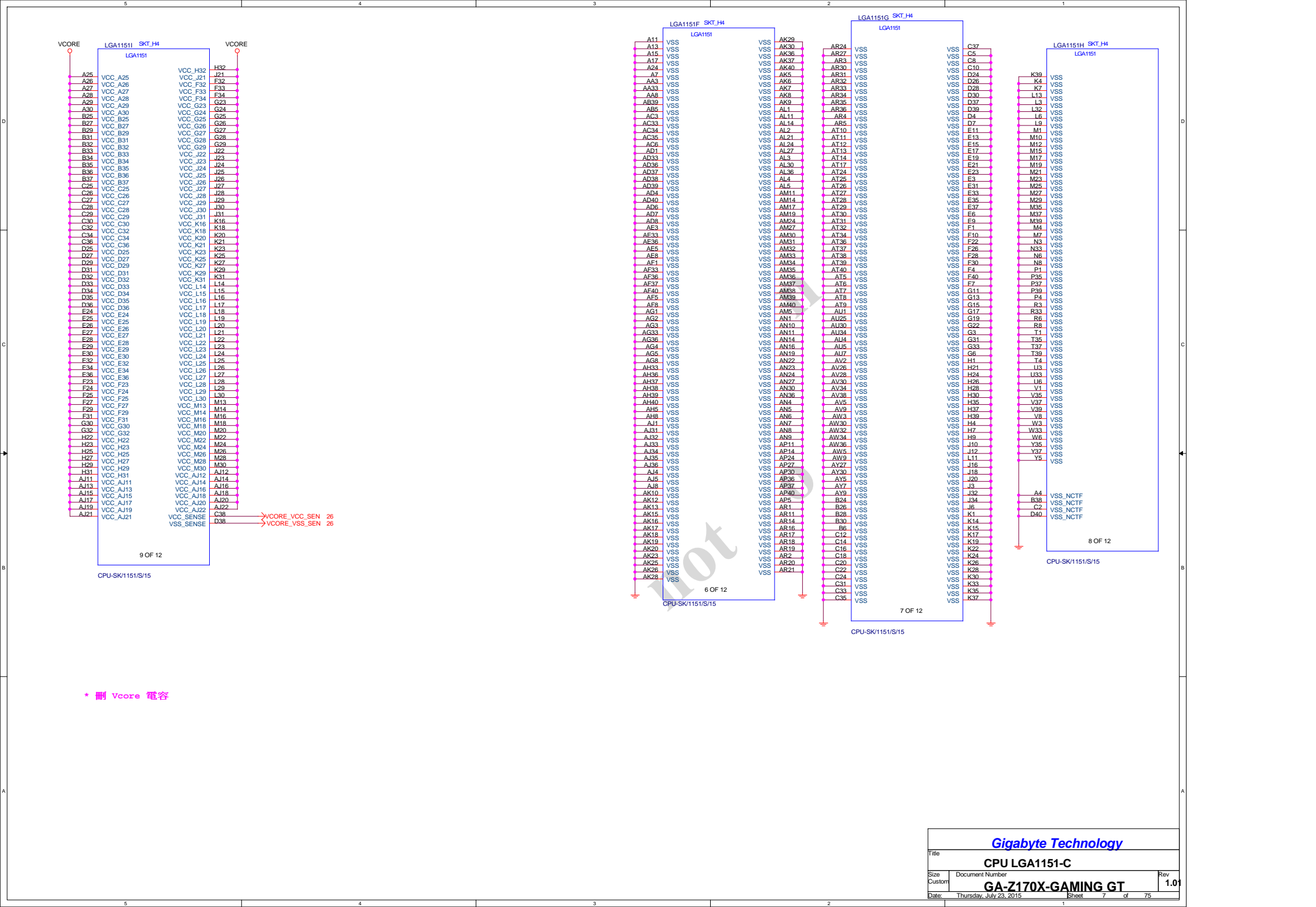
9 MAA[0..16] ↔ MAA[0..16]

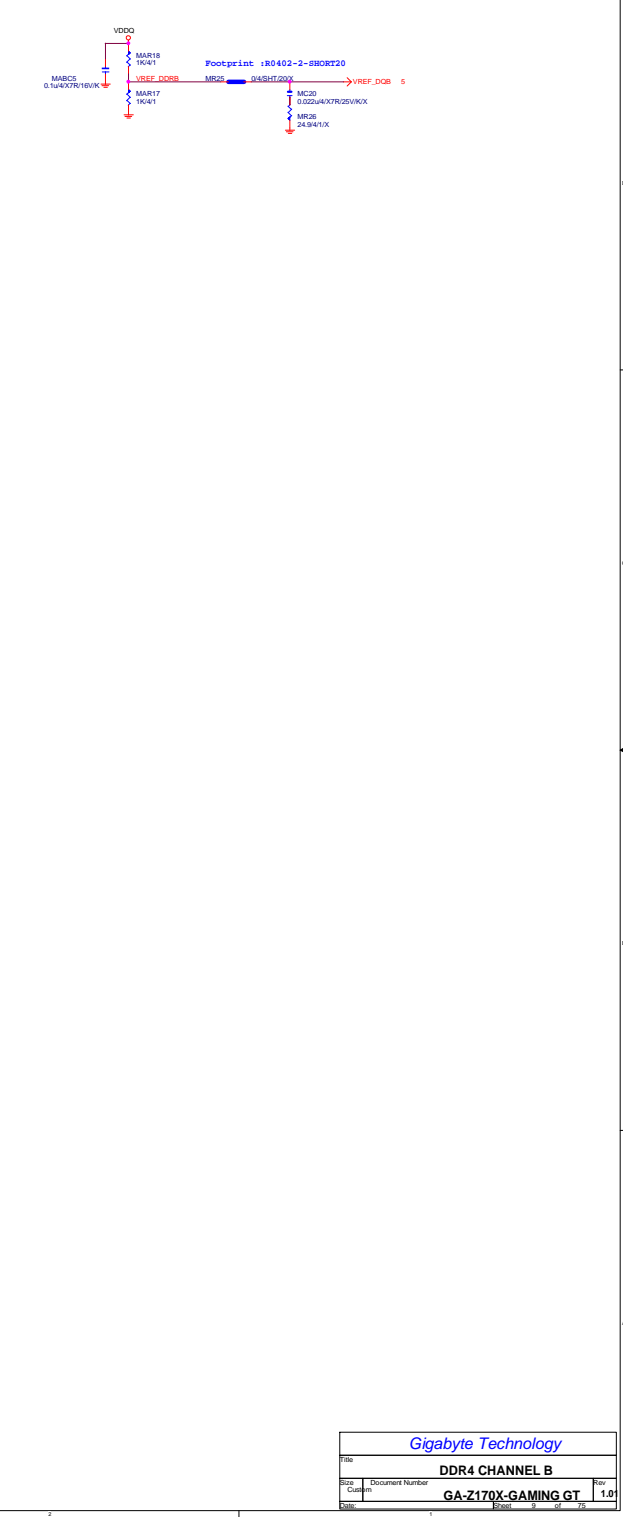
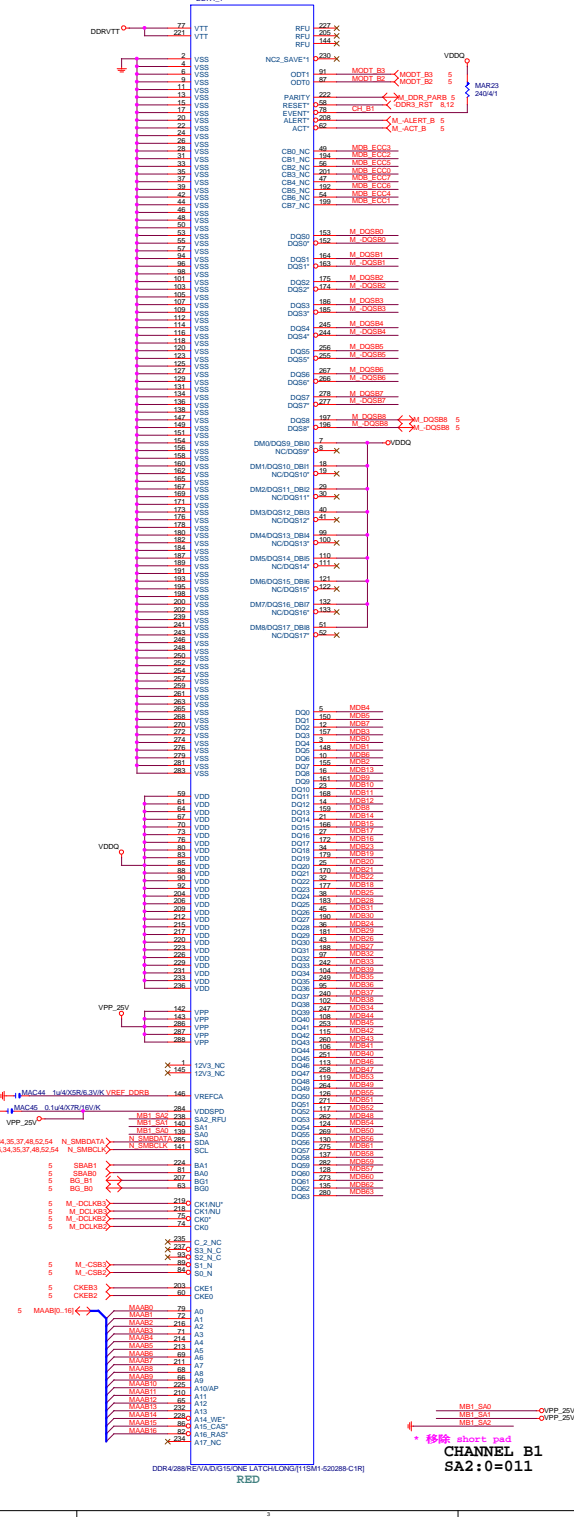
9 M_DQSB[0..7] ↔ M_DQSB[0..7]

9 M_DQSB[0..7] ↔ M_DQSB[0..7]

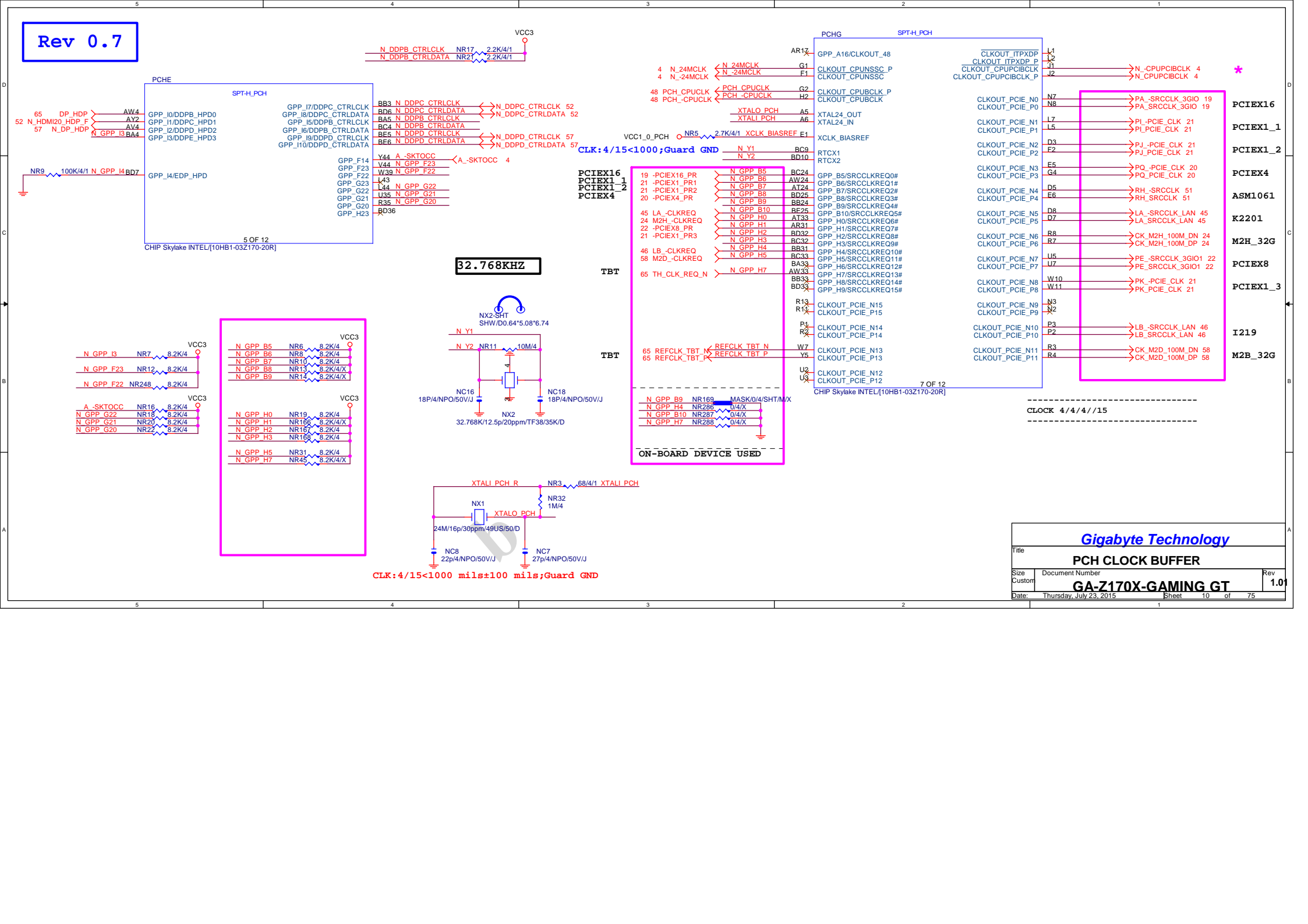
Gigabyte Technology

Title			CPU LGA1151-B		
Size			Document Number		
Custom			GA-Z170X-GAMING GT		
Date:			Thursday, July 23, 2015		
			Sheet 5 of 75		
			Rev 1.01		

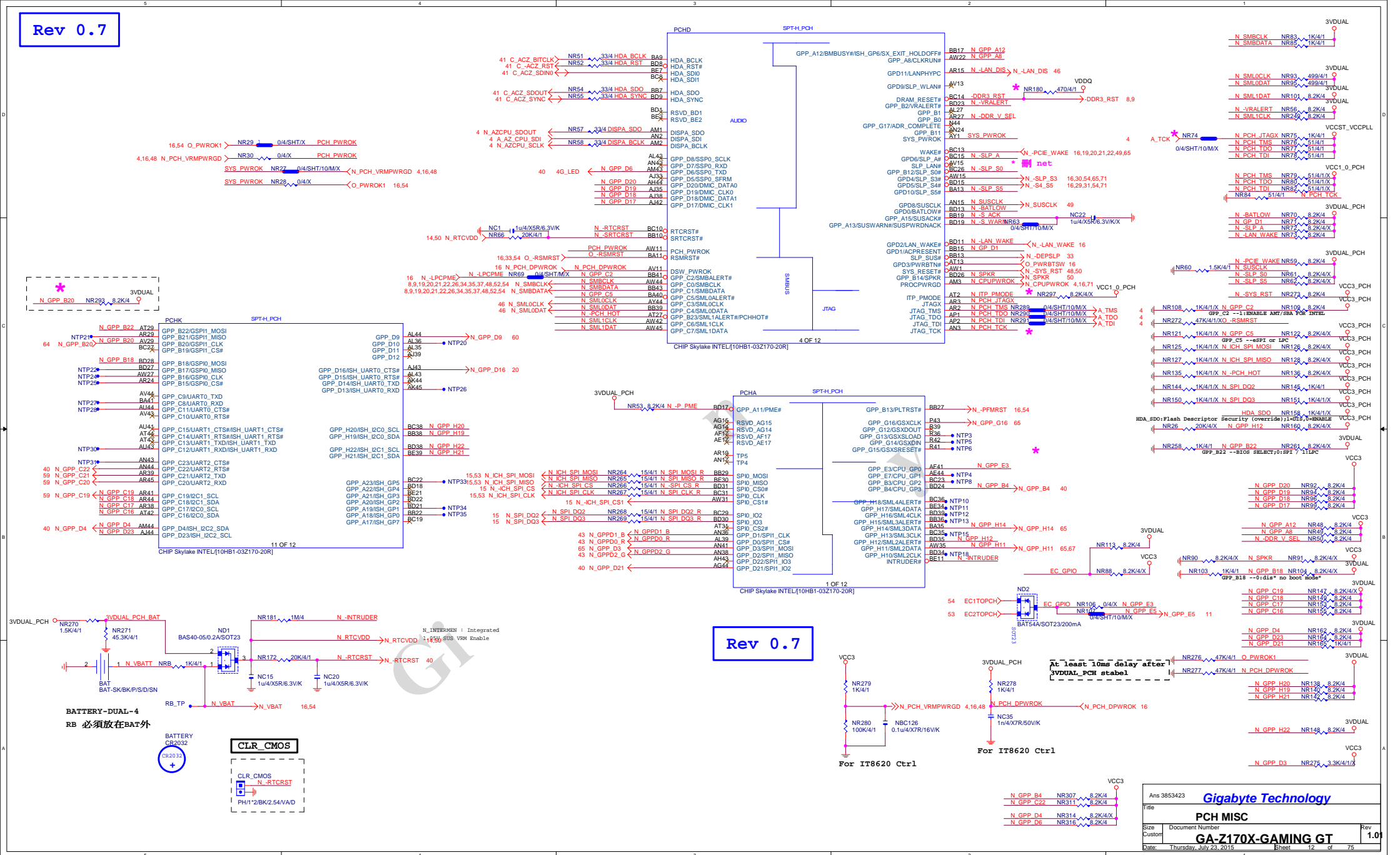




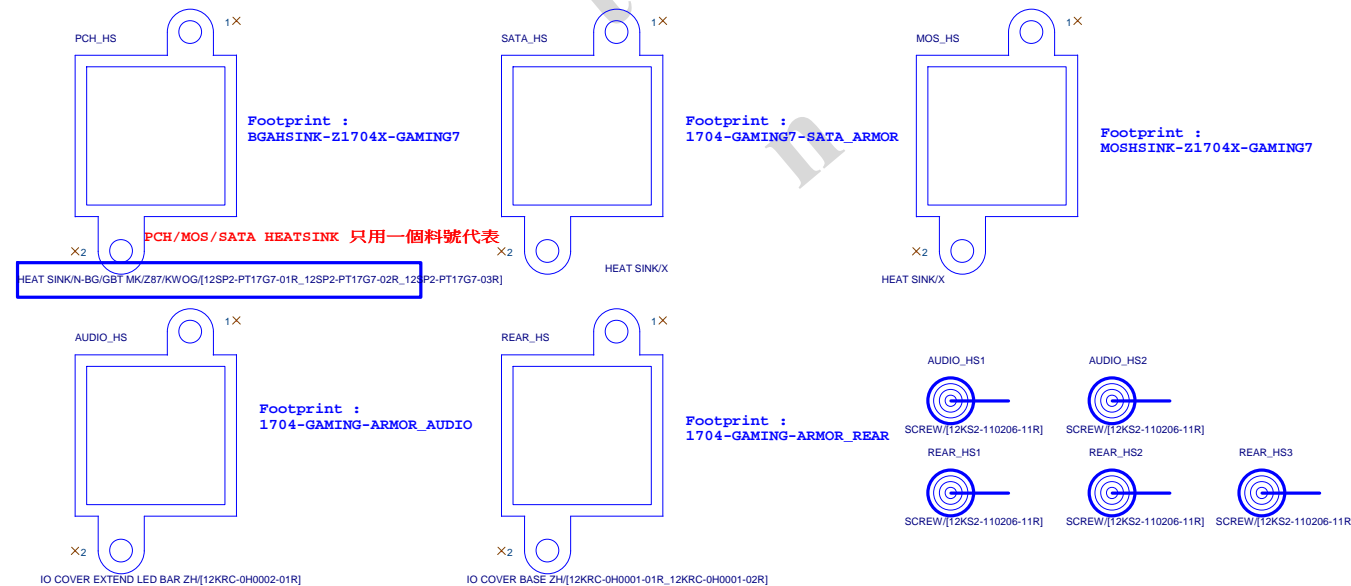
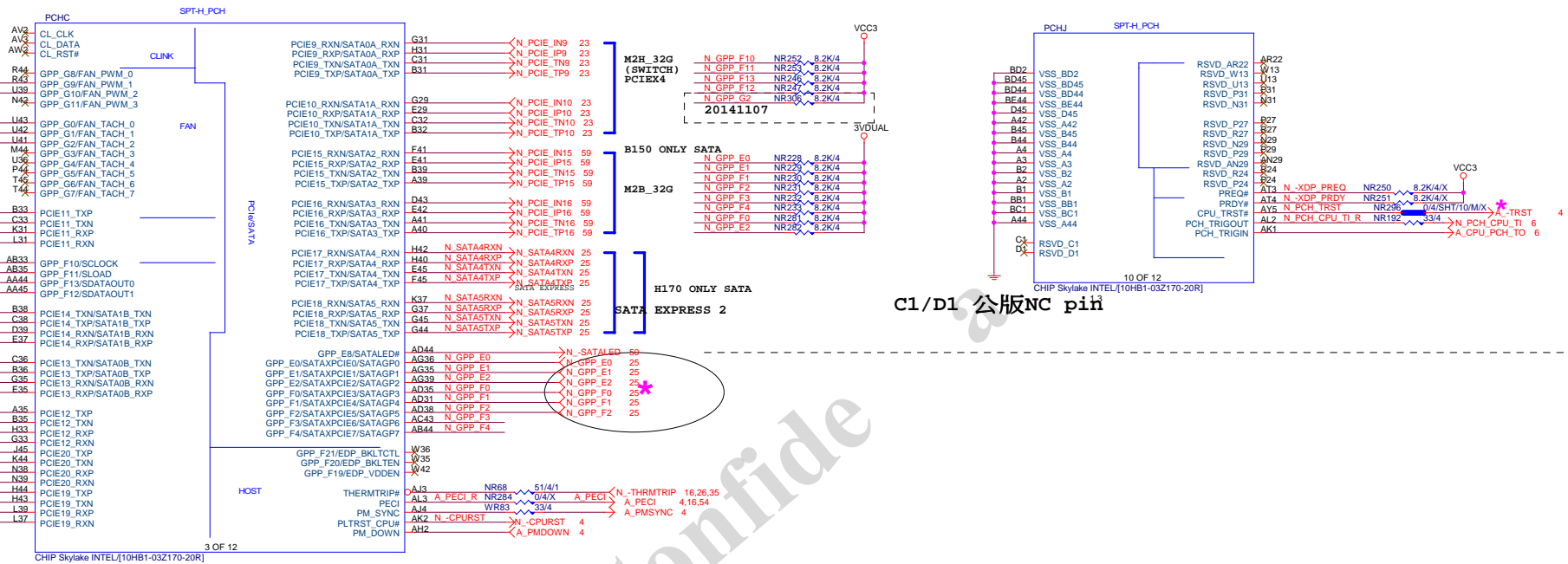
Rev 0.7

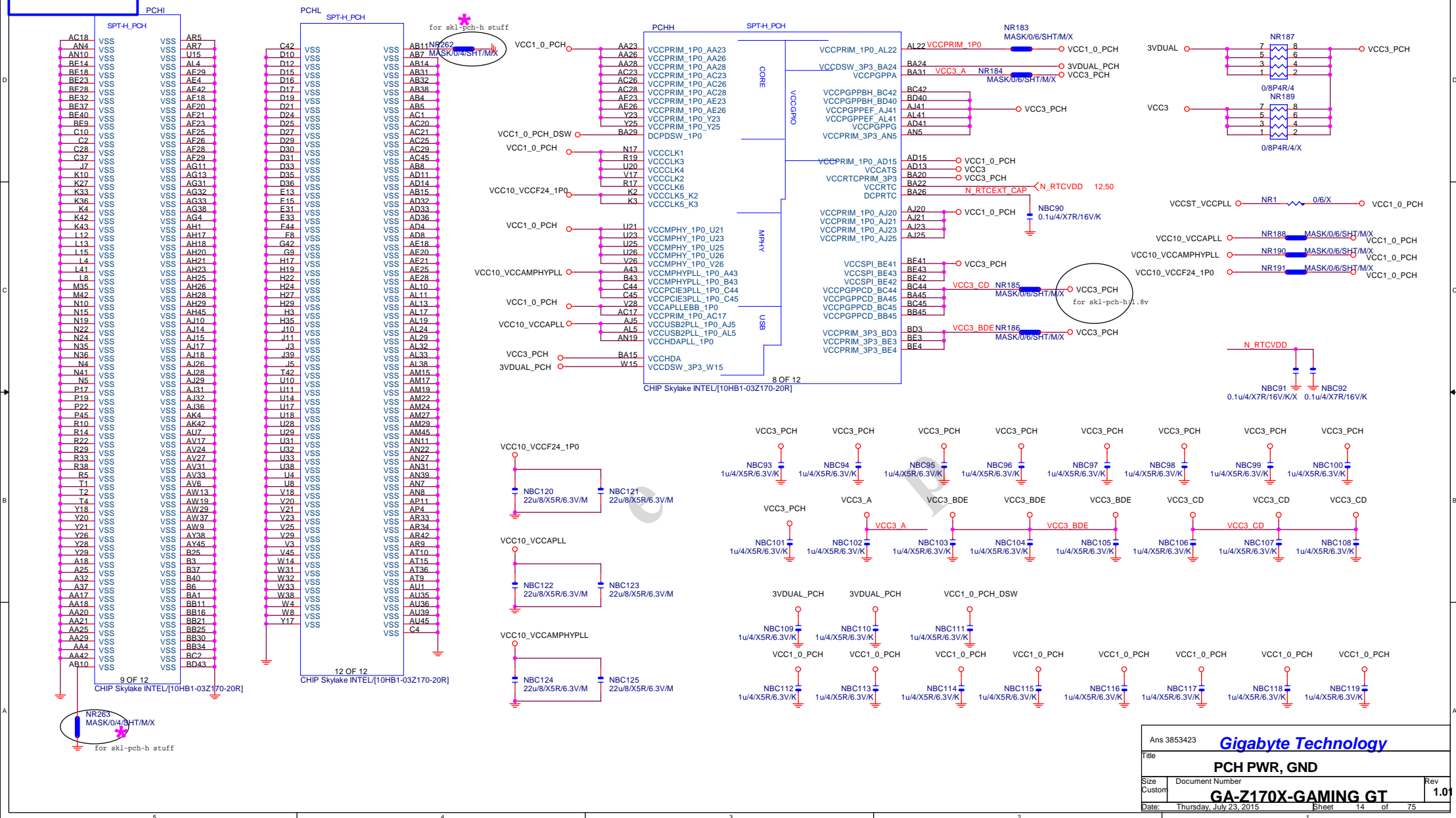




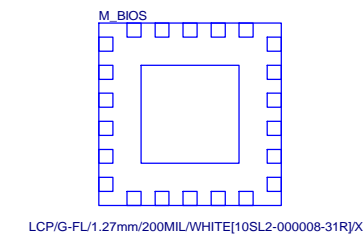
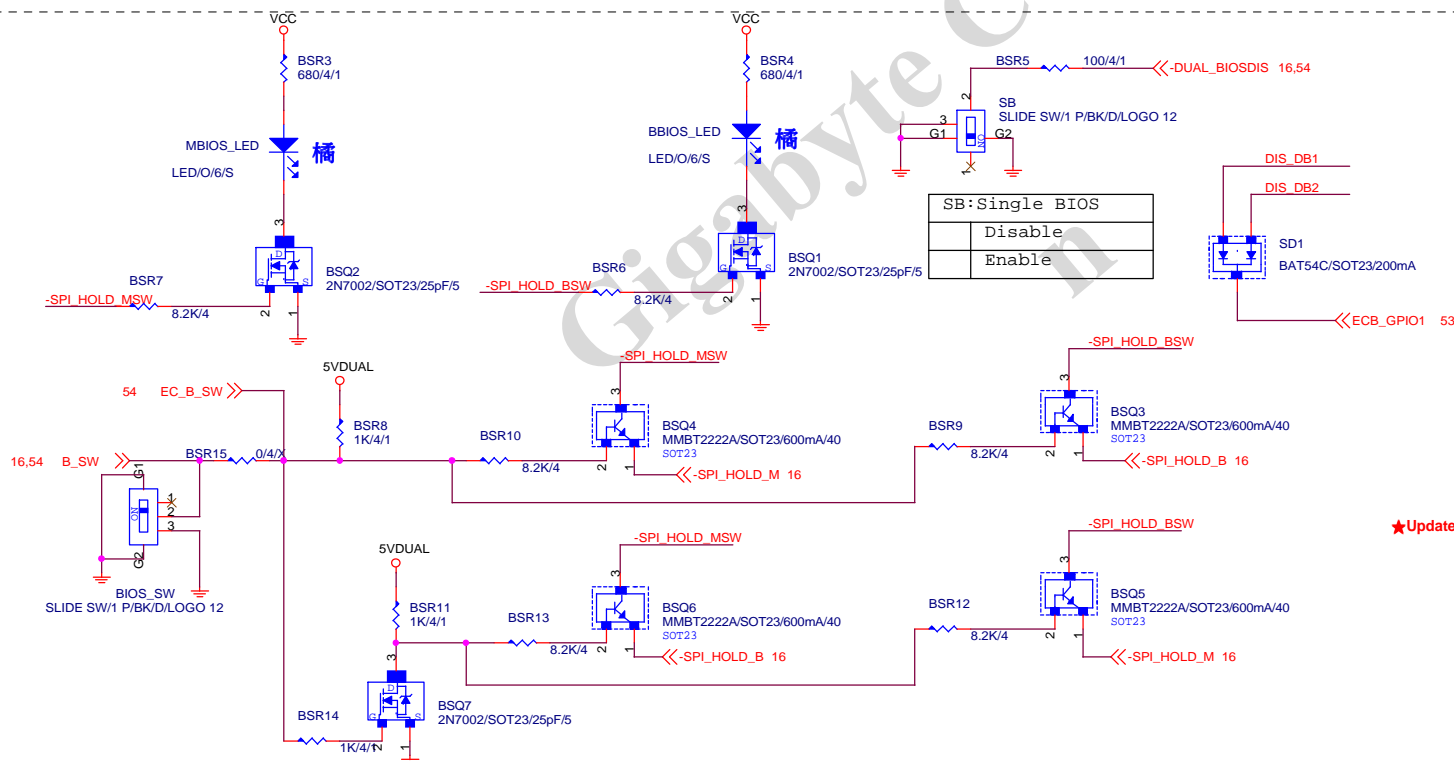
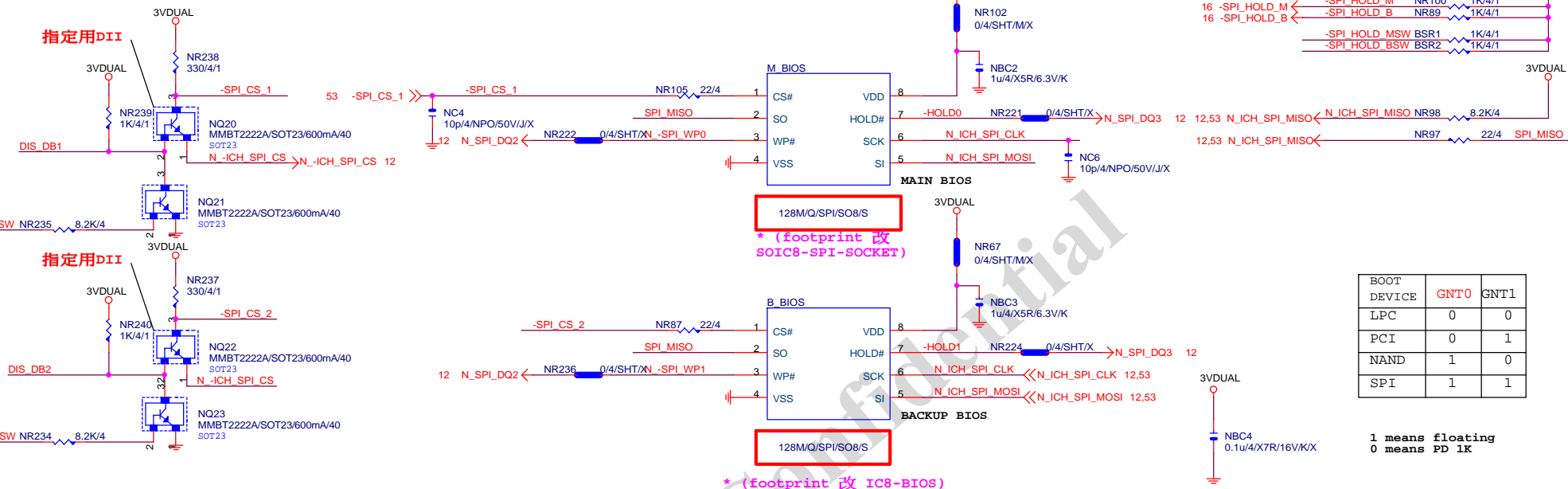


裝甲HEATSINK 分成五大部份



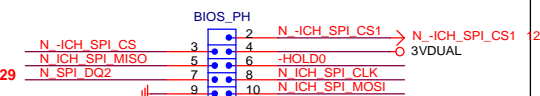


指定用DII



* 試産先上, PVT 移除

BIOS_PH



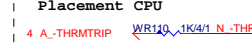
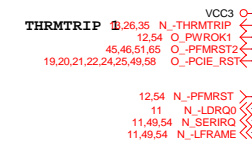
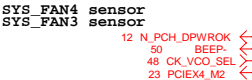
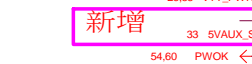
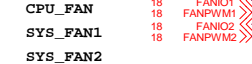
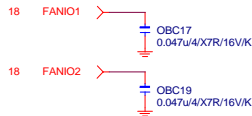
Footprint the same, confirmed by Graceing.

Use COM port pin header part.

Gigabyte Technology

Title	BIOS	
Size	Document Number	GA-Z170X-GAMING GT
Custom		Rev 1.01
Date:	Thursday, July 23, 2015	Sheet 15 of 75

SIO IT8628BX REV:1.07

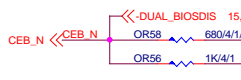


CPU 端 A-THRMTRIP不可與PCH及SIO N-THRMTRIP直接連接。否則會出現無法拉Low情況。

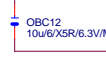
FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP1	YES PIN56

IT8620E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時會拉 Lo
PIN 90/91	DEFAULT為HDLed FUNCTION GP93 BYPASS TO GP92 高溫時 GP92 會被拉Lo(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 Lo
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用,不然會互相干擾
PIN 22	PIN22, 需高於3V, 若低於 接部分COM PORT及安裝線場區會異常動作。

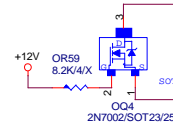
DUAL BIOS OPT STRAP



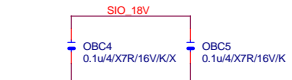
SIO CAP



Power leakage



SIO_18V



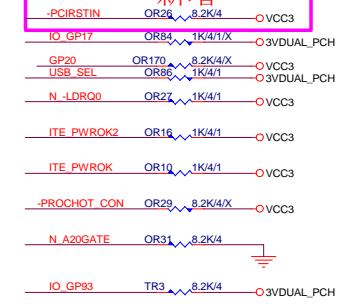
CLOSE SIO PIN4 VREF_25

MB ID

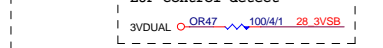
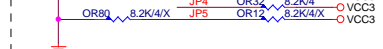


PWR SHT

SIO PU

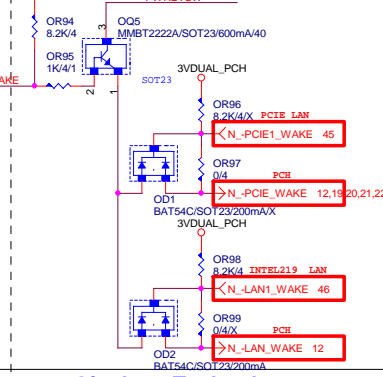


SIO STRAP

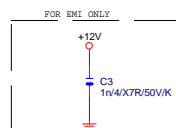
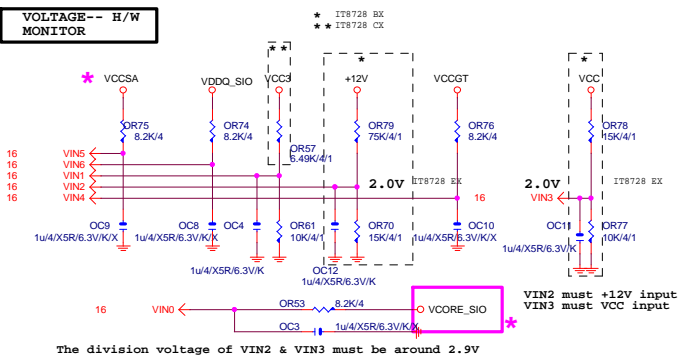
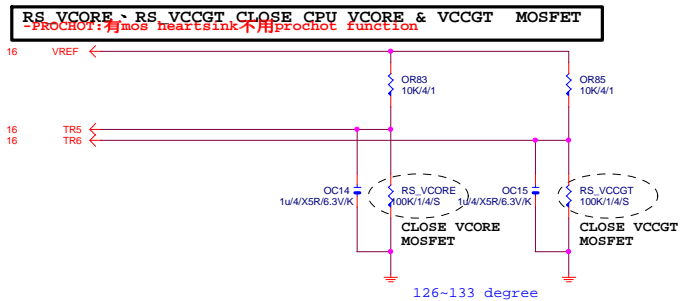
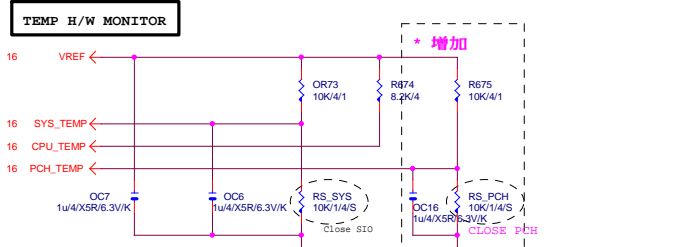


JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual BIOS CS PIN Disable
JP3	0	Dual BIOS CS PIN Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

Dual LAN (組態三)



Gigabyte Technology	
Title	ITE 8620 LPC IO
Size	Document Number
Custom	GA-Z170X-GAMING
Date	Thursday, July 23, 2015
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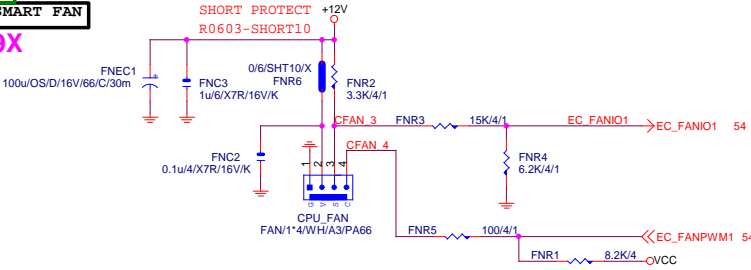
**Gigabyte Technology**

Title			HWM,KB/MS, FAN CTRL
Size	Document Number		Rev
Custom	GA-Z170X-GAMING GT		1.01
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Rev: 0.4

CPU SMART FAN

IT879X

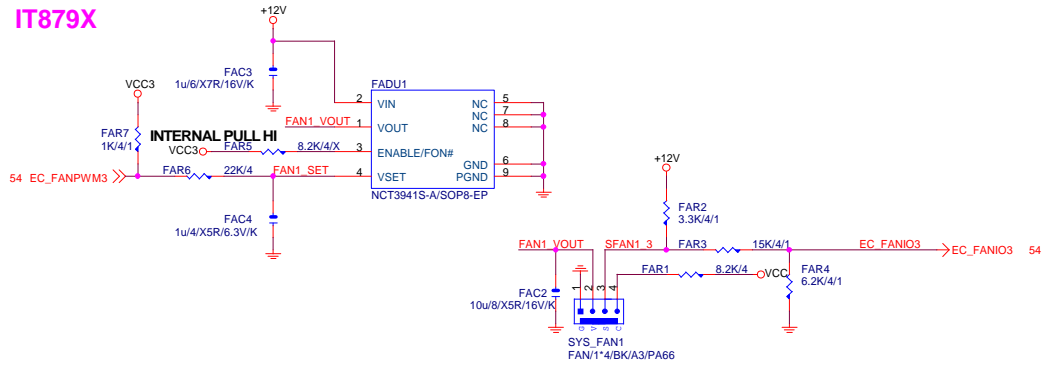


SYSTEM FAN1

Linear SYS_FAN

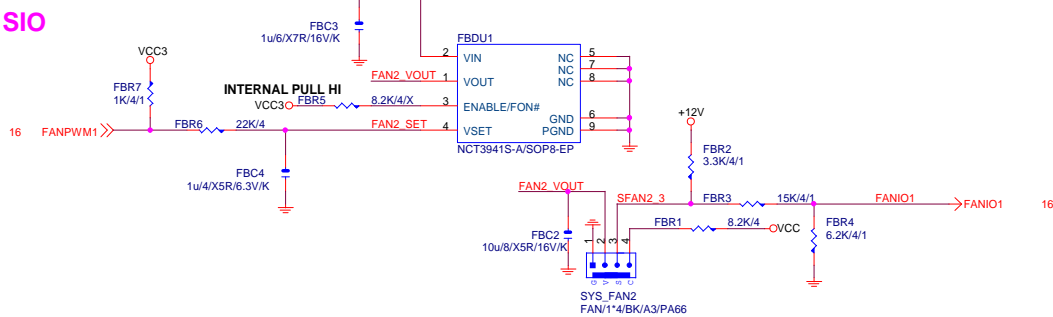
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)

IT879X



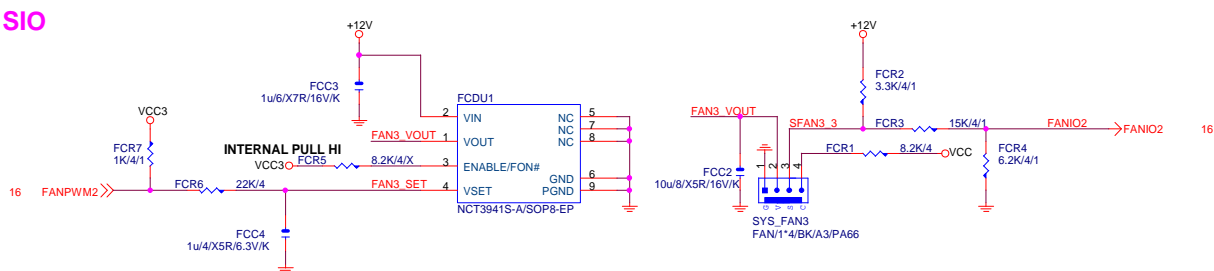
SYSTEM FAN2

SIO



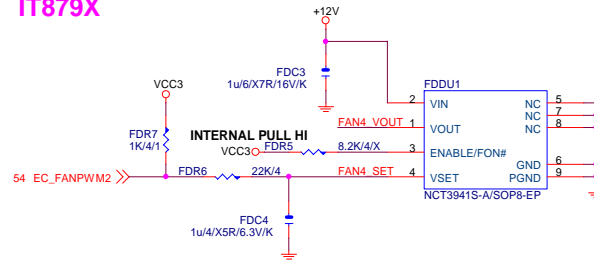
SYSTEM FAN3

SIO



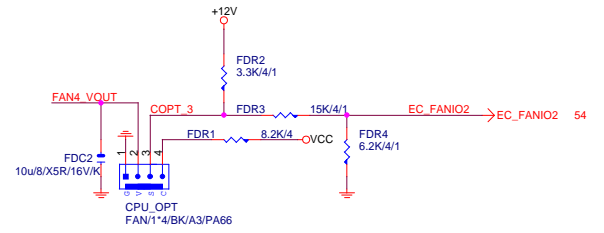
CPU_OPT

IT879X

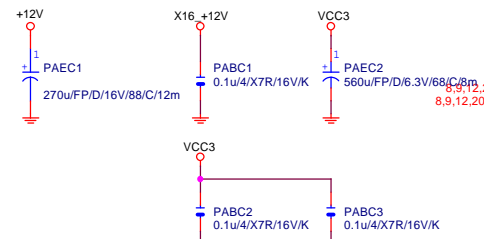


SYSTEM FAN4

SIO

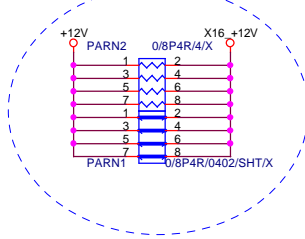


PCIEX16 CAP



PCIEX16 PROTECT SHT

+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHZ*(8b/10b)=2Gb/s=250MB/s

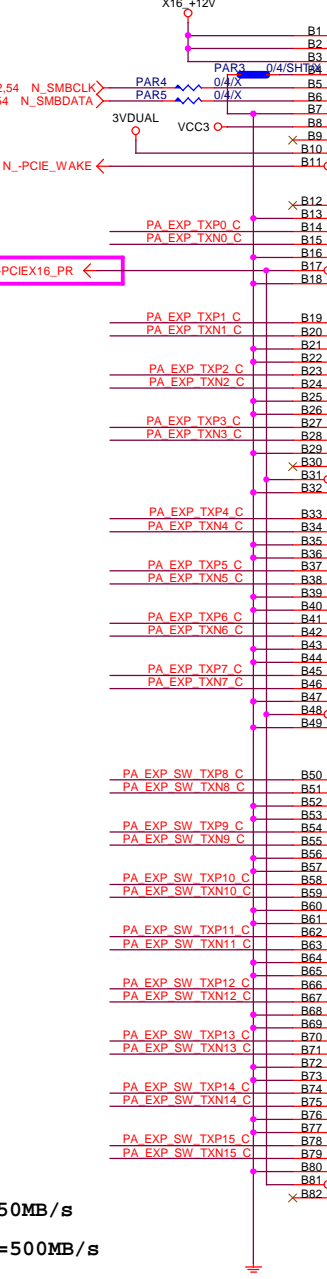
PCE-E X1(雙向) BANDWITH=2.5GHZ*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHZ*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHZ*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCIEX16 SLOT



PCIESLOT-164STH



PCI-E/16X-164P/RE/LONG DOUBLE/HK*2/SHELL(11AC1-023164-E1R)

紅色

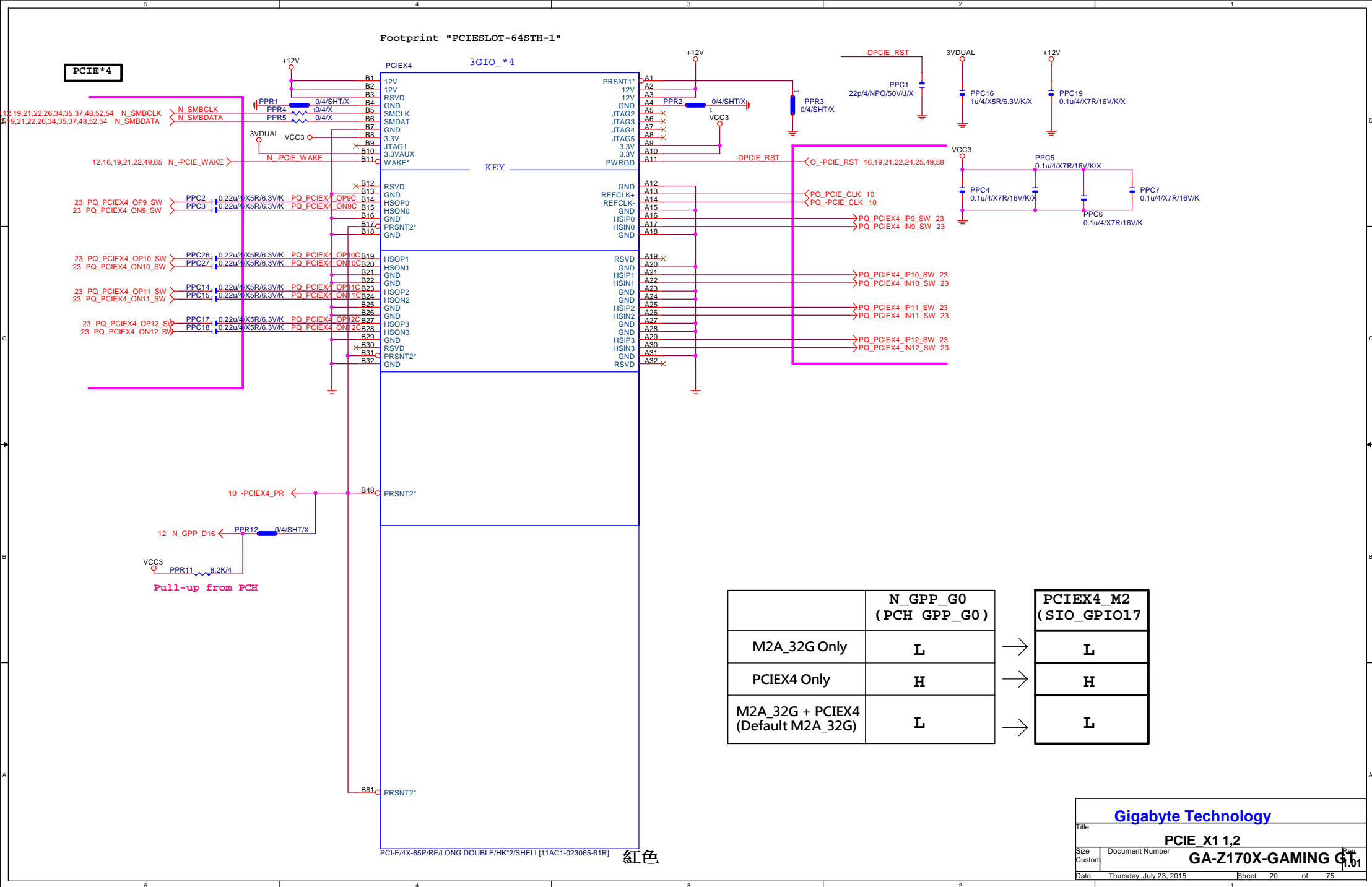
PCIEX16:16/5/5/5/16

PA EXP RXP0.15]	>>>PA_EXP_RXP0[0..15]	4,23
PA EXP RXN0.15]	>>>PA_EXP_RXN0[0..15]	4,23
PA EXP TXP0.15]	>>>PA_EXP_TXP0[0..15]	4,23
PA EXP TXN0.15]	>>>PA_EXP_TXN0[0..15]	4,23
PA EXP SW RXP8.15]	>>>PA_EXP_SW_RXP8[8..15]	23
PA EXP SW RXN8.15]	>>>PA_EXP_SW_RXN8[8..15]	23
PA EXP SW TXP8.15]	>>>PA_EXP_SW_TXP8[8..15]	23
PA EXP SW TXN8.15]	>>>PA_EXP_SW_TXN8[8..15]	23

Gigabyte Technology

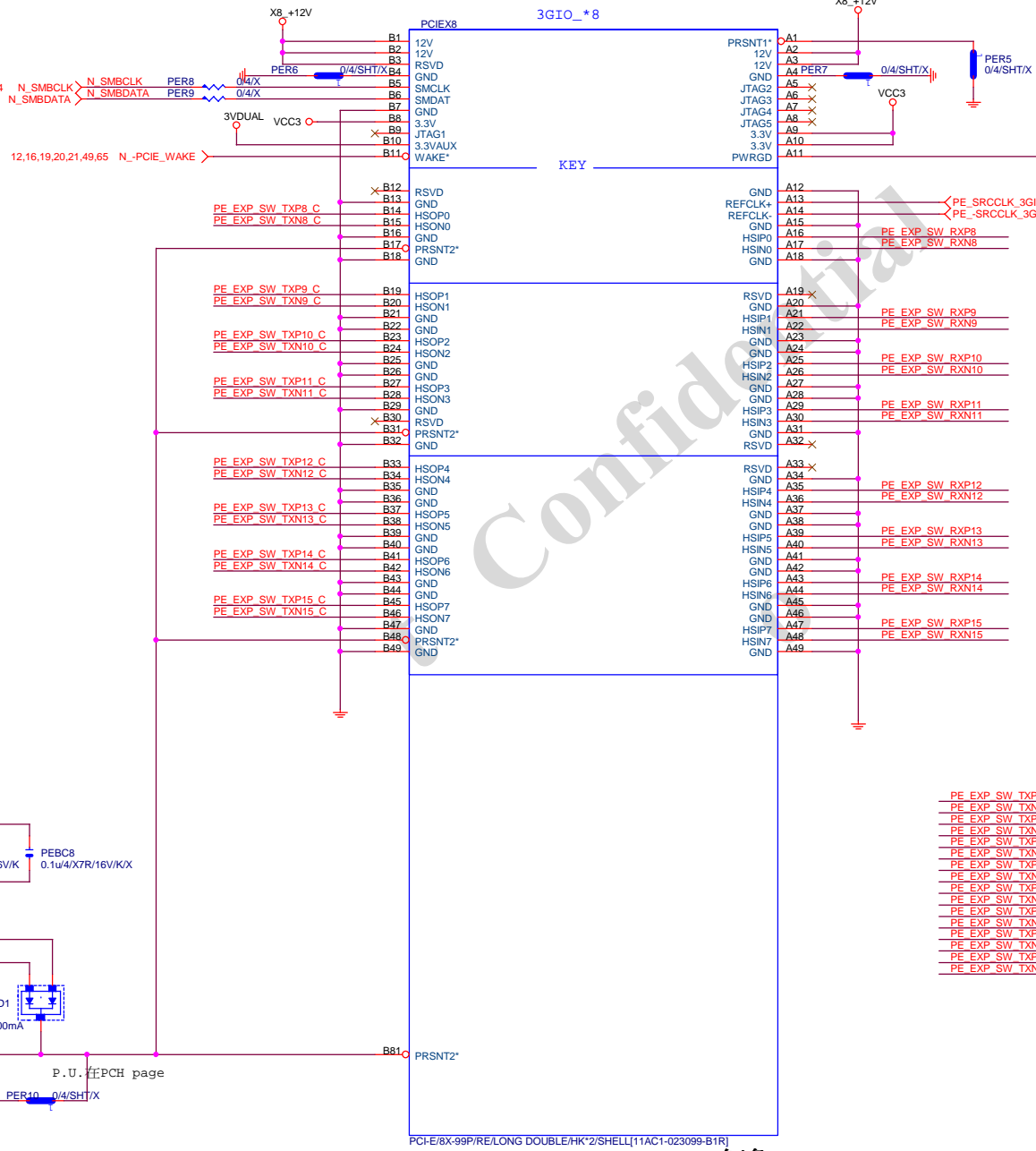
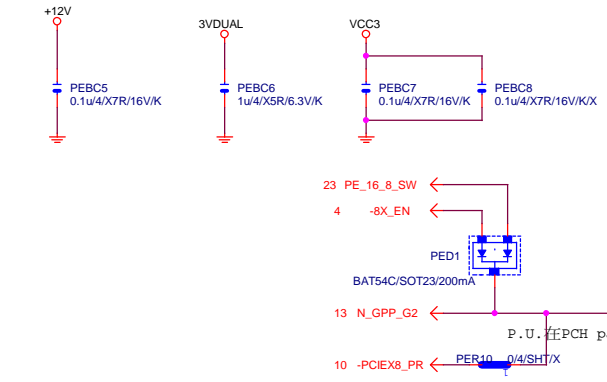
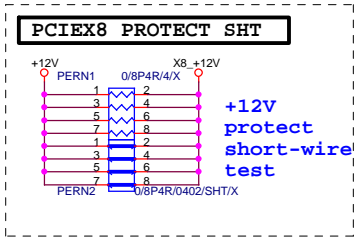
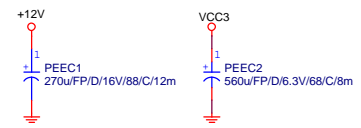
PCI EXPRESS * 16

Title	Document Number	Rev
Size	GA-Z170X-GAMING G1.01	1.01
Date:	Thursday, July 23, 2015	Sheet 19 of 75



[illegible]

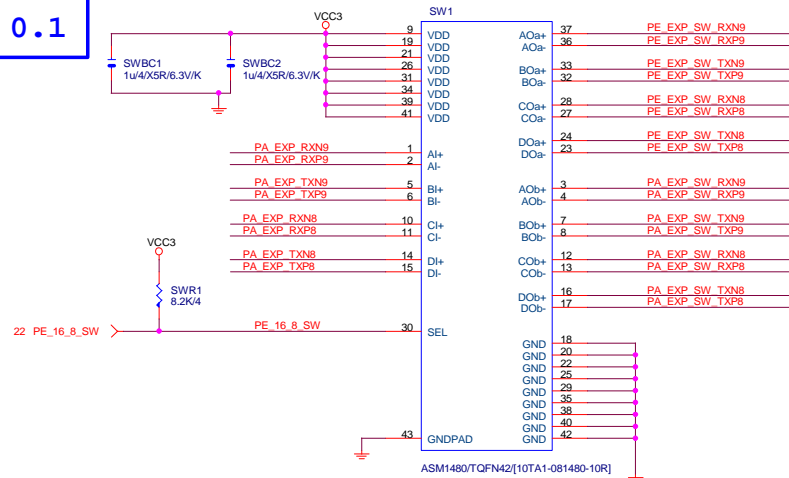
Title			
PCIE_X1 1,2			
Size	Document Number	Rev	
Custom	GA-Z170X-GAMING GT	1.01	
Date:	Thursday, July 23, 2015	Sheet	21 of 75



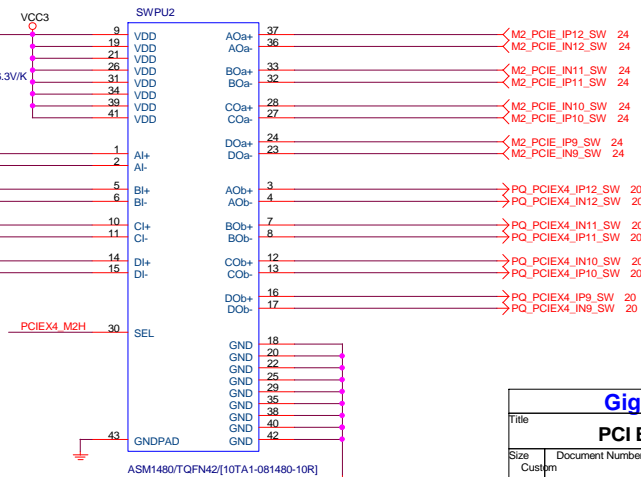
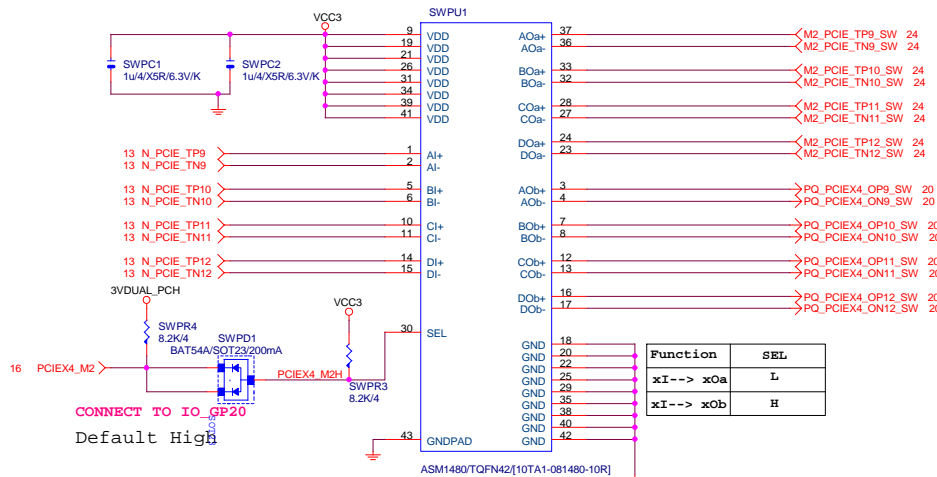
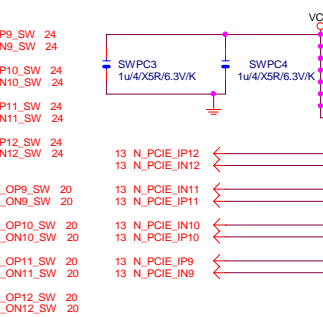
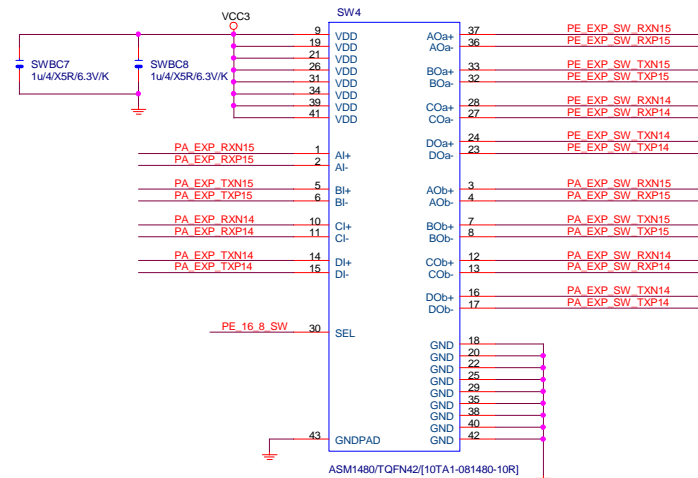
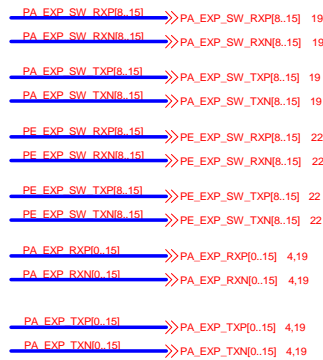
PE_EXP_SW_RXP[8..15] >> PE_EXP_SW_RXP[8..15] 23
PE_EXP_SW_RXN[8..15] >> PE_EXP_SW_RXN[8..15] 23
PE_EXP_SW_TXP[8..15] >> PE_EXP_SW_TXP[8..15] 23
PE_EXP_SW_TXN[8..15] >> PE_EXP_SW_TXN[8..15] 23

PE_EXP_SW_TXP8	PEC7	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP8_C
PE_EXP_SW_TXN8	PEC8	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN8_C
PE_EXP_SW_TXP9	PEC9	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP9_C
PE_EXP_SW_TXN9	PEC10	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN9_C
PE_EXP_SW_TXP10	PEC11	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP10_C
PE_EXP_SW_TXN10	PEC12	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN10_C
PE_EXP_SW_TXP11	PEC13	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP11_C
PE_EXP_SW_TXN11	PEC14	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN11_C
PE_EXP_SW_TXP12	PEC15	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP12_C
PE_EXP_SW_TXN12	PEC16	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN12_C
PE_EXP_SW_TXP13	PEC17	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP13_C
PE_EXP_SW_TXN13	PEC18	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN13_C
PE_EXP_SW_TXP14	PEC19	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP14_C
PE_EXP_SW_TXN14	PEC20	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN14_C
PE_EXP_SW_TXP15	PEC21	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXP15_C
PE_EXP_SW_TXN15	PEC22	0.22u4/X5R/6.3V/K	PE_EXP_SW_TXN15_C

PCI-E/8X-99P/RE/LONG DOUBLE/HK*2/SHELL[11AC1-023099-B1R]
RED 紅色



Function	SEL
xI--> xOa	L
xI--> xOb	H



Gigabyte Technology

PCI EXPRESS X16 SWITCH

Title	Document Number	Rev
Size	Custom	GA-Z170X-GAMING GT 1.01
Date:	Thursday, July 23, 2015	Sheet 23 of 75

M.2 Lane4 from PCH port18

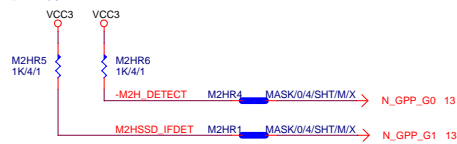
M.2 Lane3 from PCH port17

M.2 Lane2 from PCH port16

M.2 Lane2 from PCH port15

需與M2_-CLKREQ對應

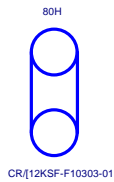
支援SATA and M.2 function



M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE X1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)	PCIE x4 (For M.2)				SATA	SATA
		SATA Express (Low)	PCIE x4 (For M.2)				SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	PCIE x4				SATA	SATA
		SATA Express (Low)	PCIE x4				SATA Express	

黑色

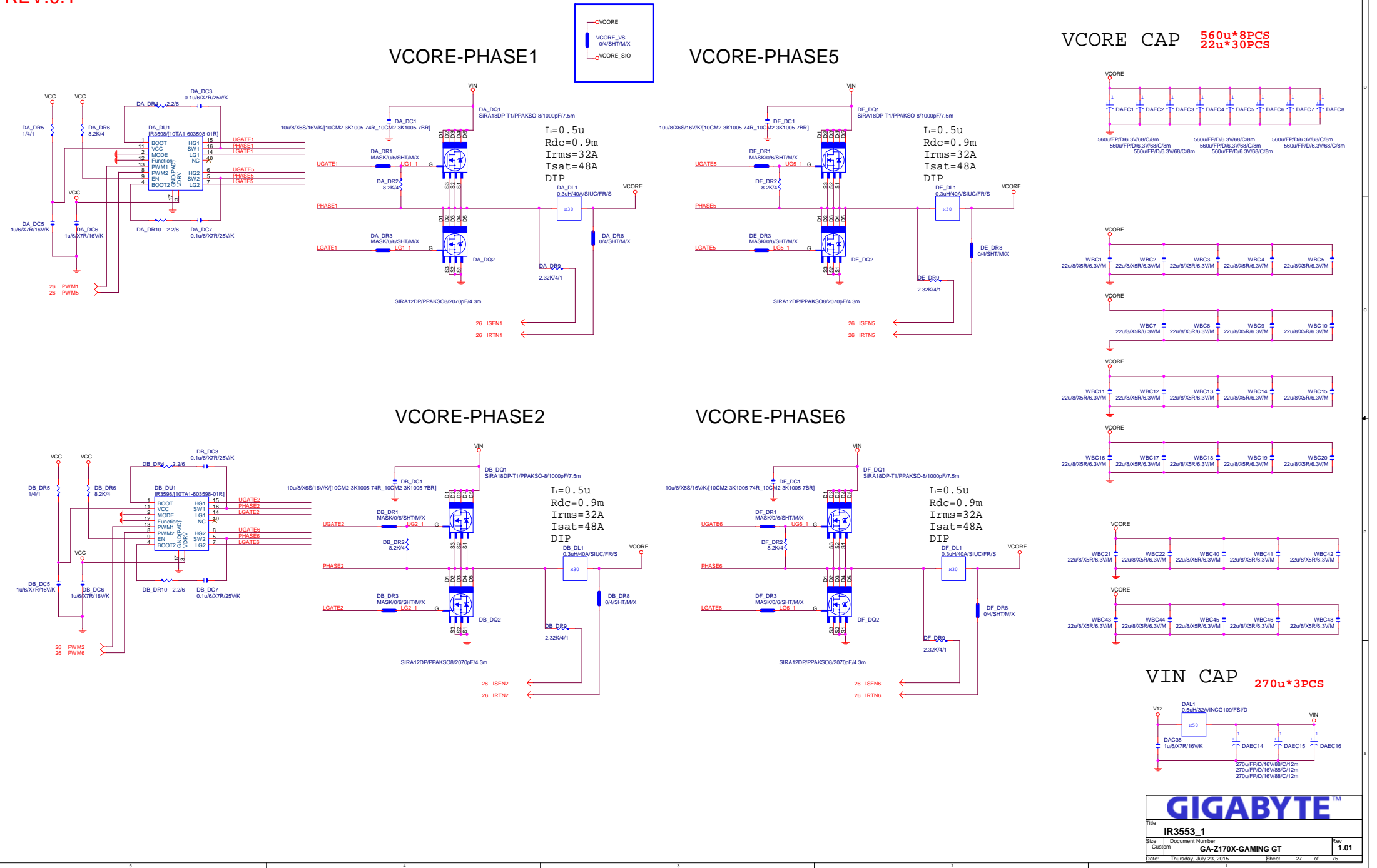
DIP螺柱



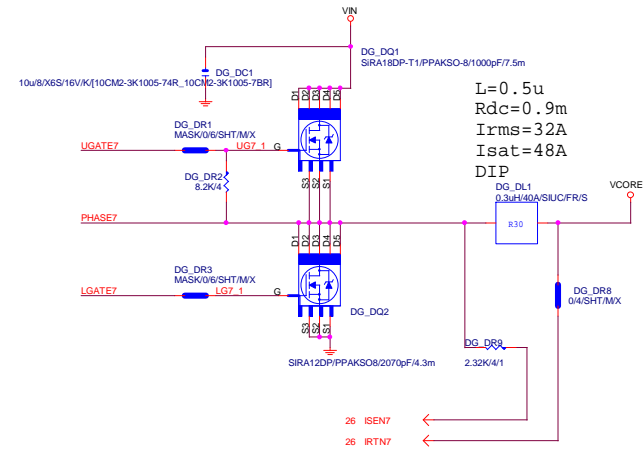
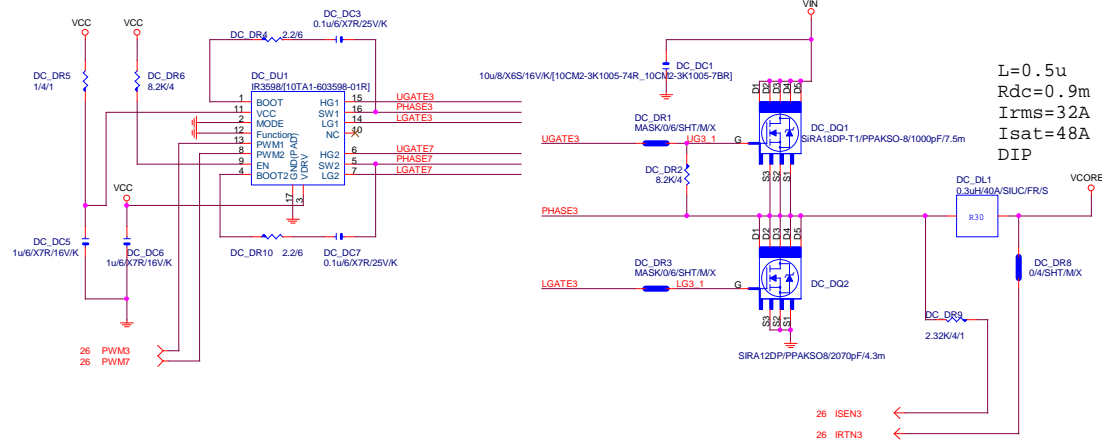
SMD螺柱



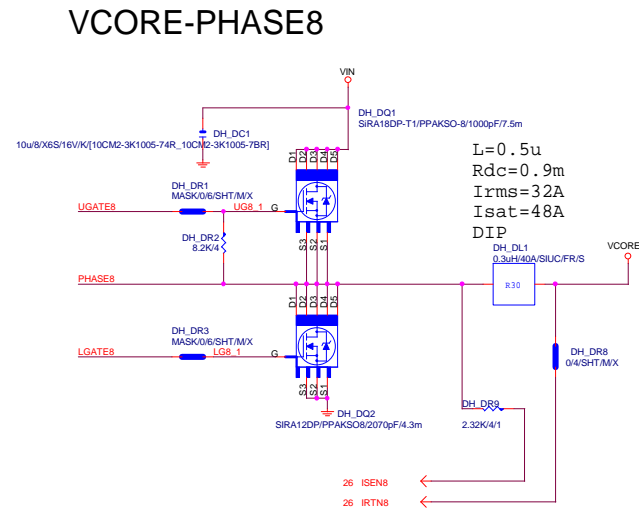
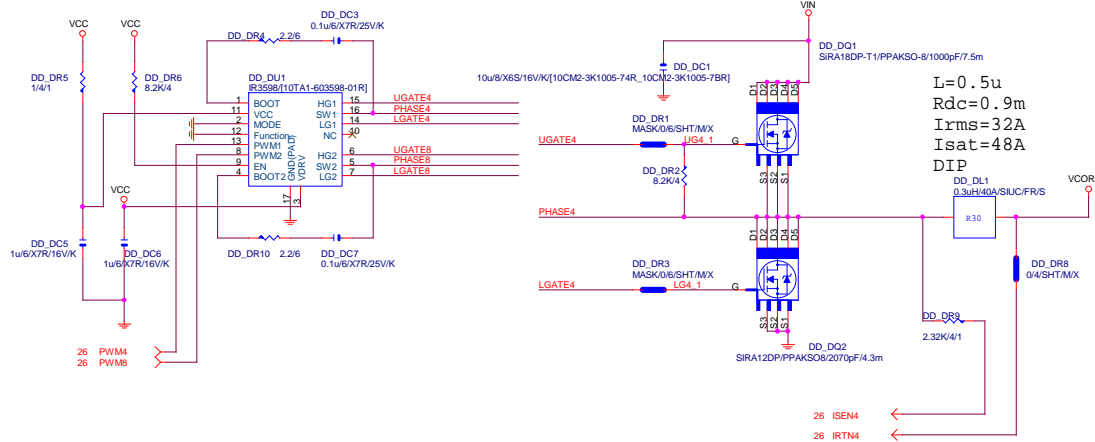




VCORE-PHASE7

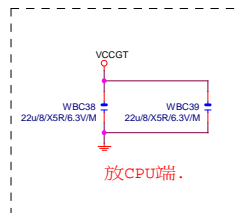
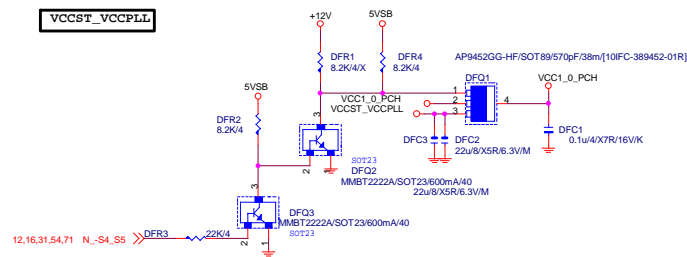


VCORE-PHASE4

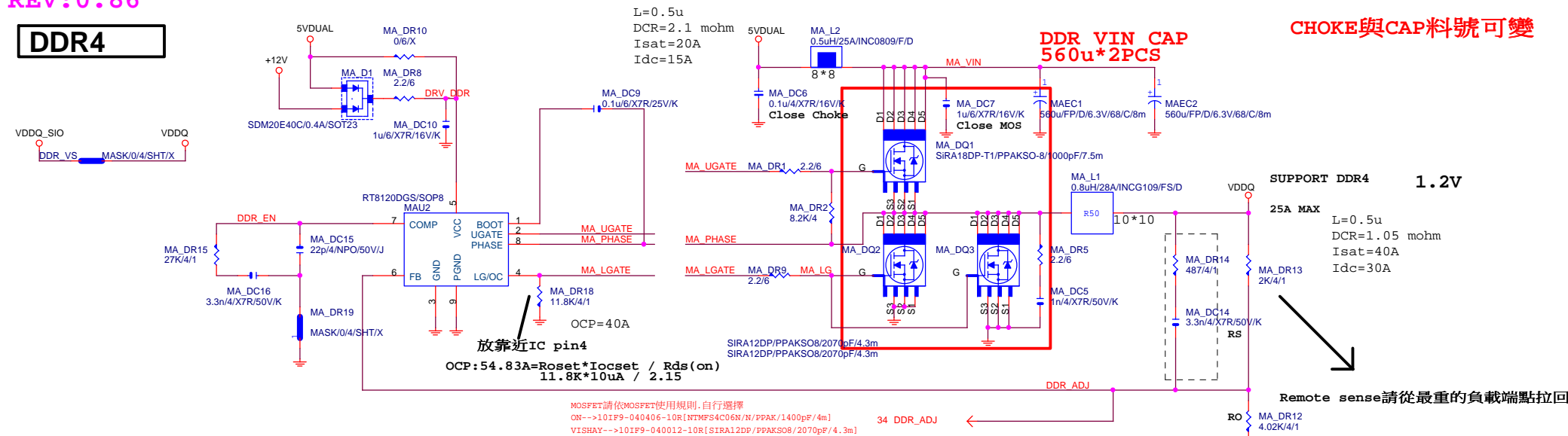


REV:0.2

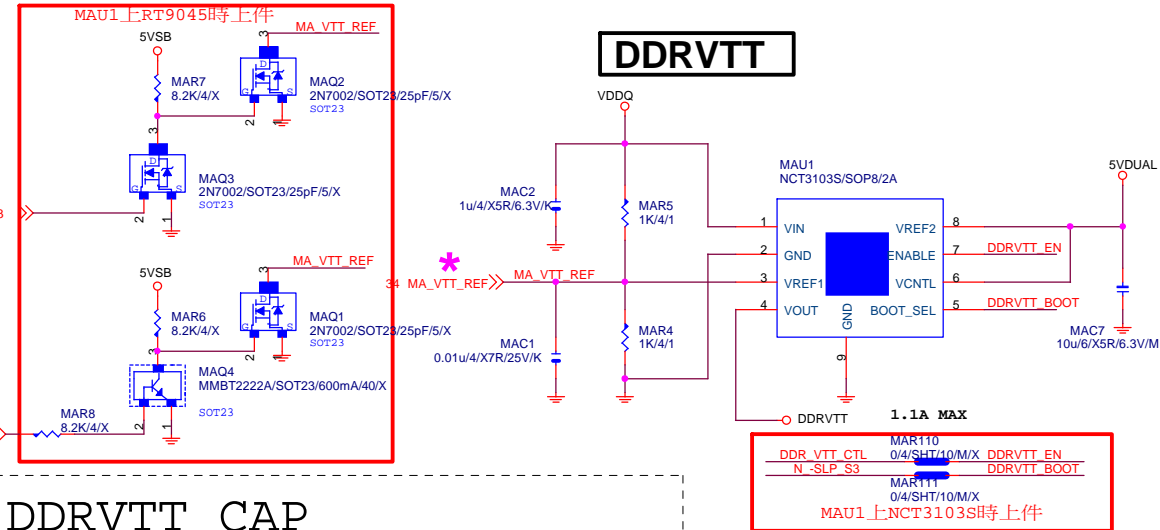
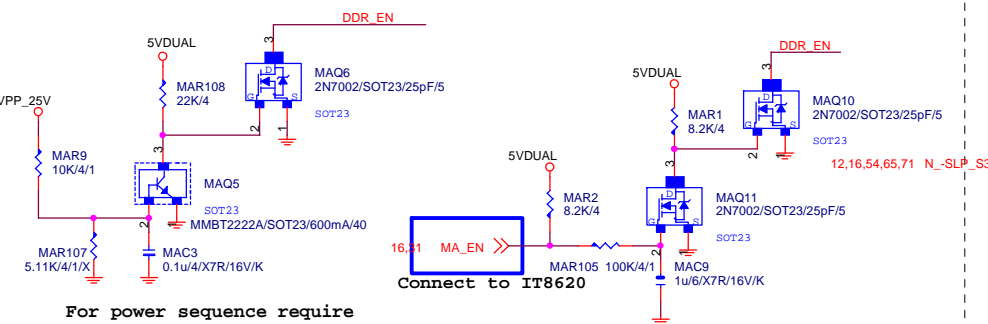
VCCST_VCCPLL



DDR4



PWR SEQ



GIGABYTE™

Title		
RT8120_DDR4 POWER		
Size	Document Number	Rev
Custom	GA-Z170X-GAMING GT	1.01
Date:	Thursday, July 23, 2015	Sheet 30 of 75

VPP 25V

CHOKES與CAP料號可變

L=0.5u
DCR=2.1 mohm
Isat=20A
Idc=15A

25A MAX

34 VPP25_ADJ ← VPP25_ADJ

PWR	SEQ
-----	-----

* 删除 MA_DR32

VPP CAP 560u*1PCS

* 大電容 x1

VPP, 25V

1

MAEC11
560u/FP/D/6.3V/68/C/8m

GIGABYTE™

Title
RT8120_VPP25 POWER

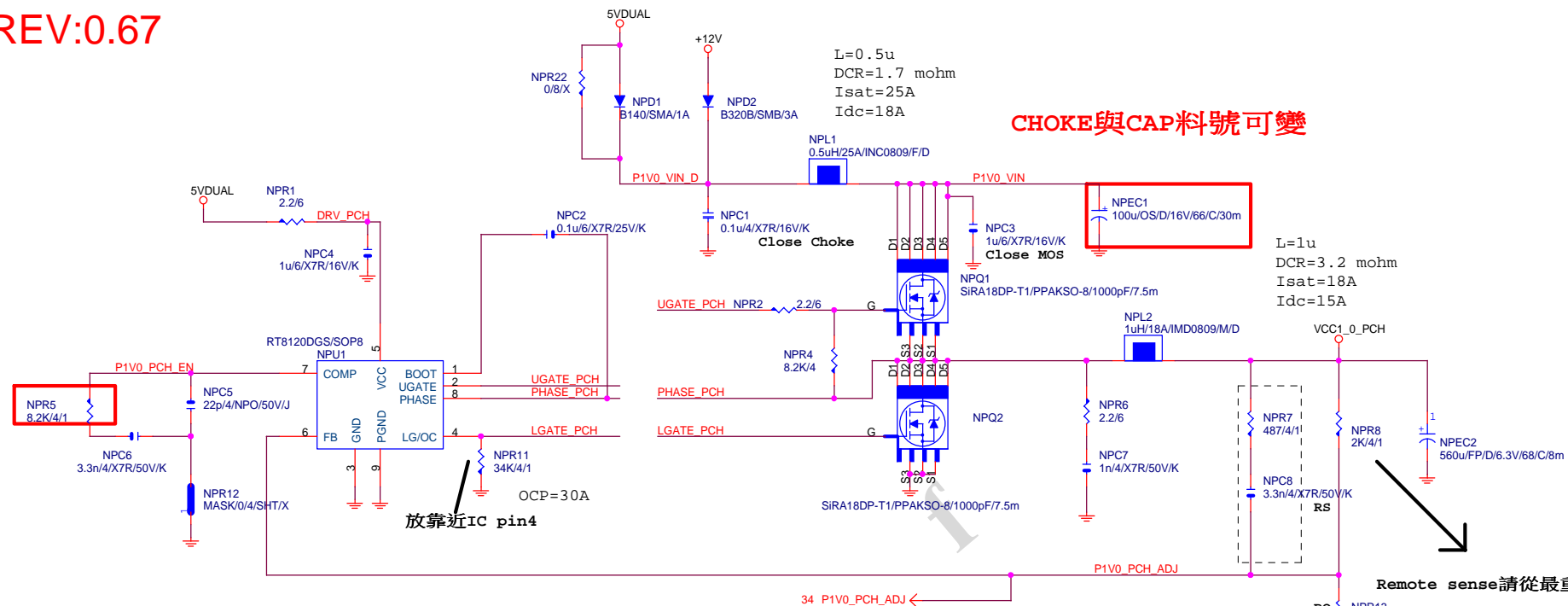
Size	Document Number
Custom	GA-Z170X-GAMING GT

Rev
1.01

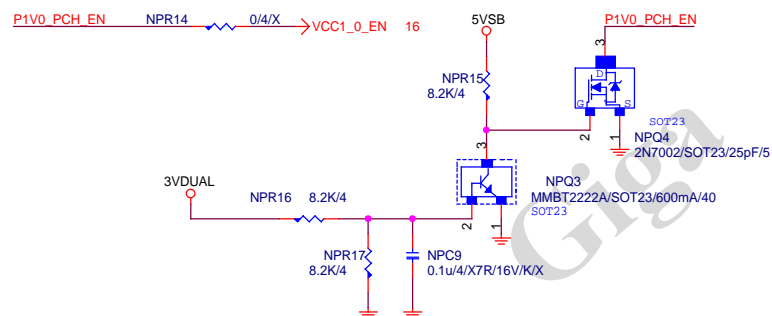
Date: Thursday, July 23, 2015

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REV:0.67



PWR_SEQ

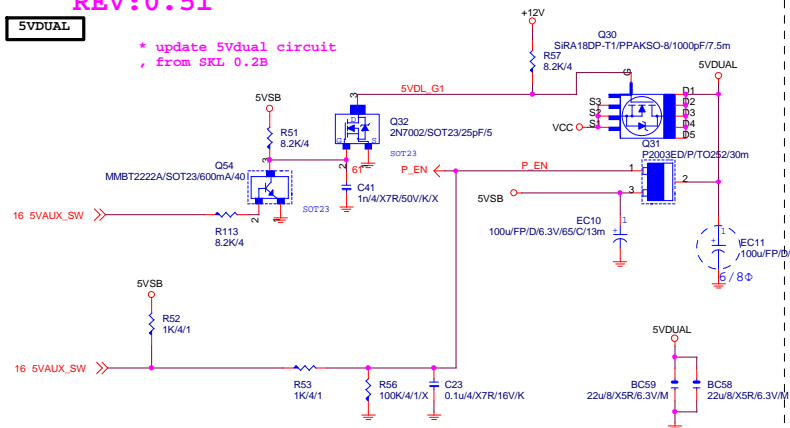


請放置CHOKE一出來的地方

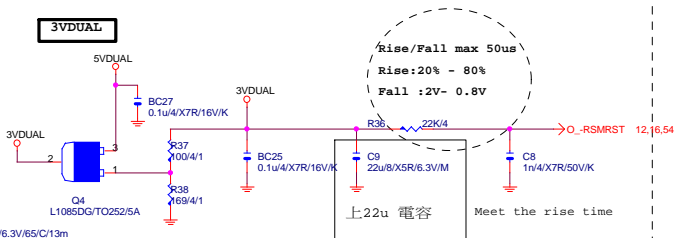
GIGABYTE™			
Title			
RT8120_PCH POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-GAMING GT	1.01	
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5VDUAL

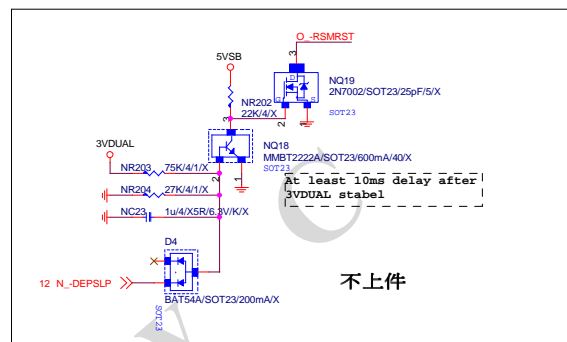
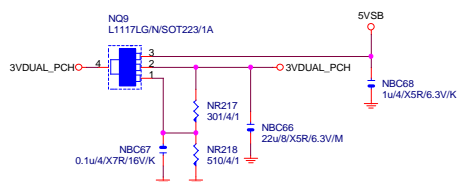
```
* update 5Vdual circuit
, from SKL 0.2B
```



3VDUAL

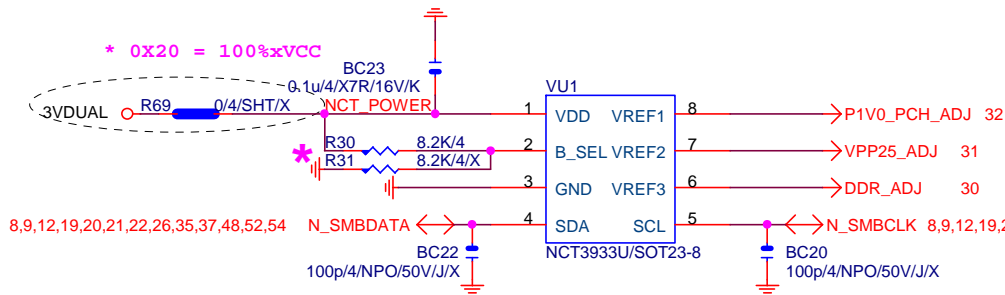


3VDUAL_PCH

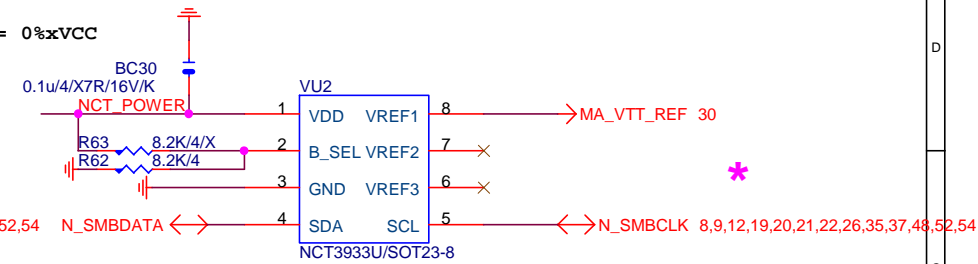


不上件

OVER VOLTAGE



0X2A = 0%xVCC

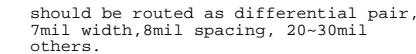


0X22 = 75%xVCC

* 删除 OVU3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

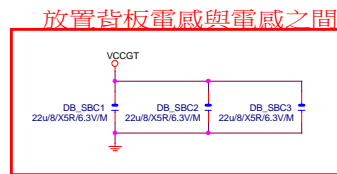
Gigabyte Technology		
Title		
CPU CORE VR-2		
Size Custom	Document Number	Rev
GA-Z170X-GAMING GT		1.01
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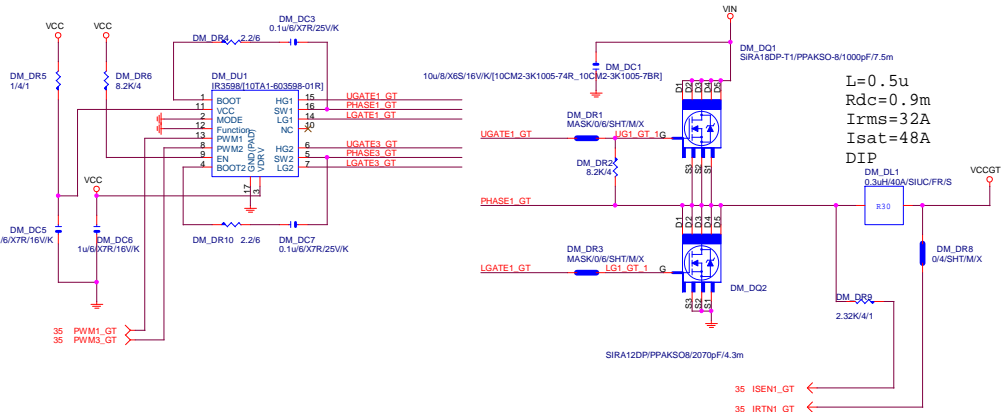
Close to VCCGT
output inductor
phasel

For Phase margin and gain margin measure

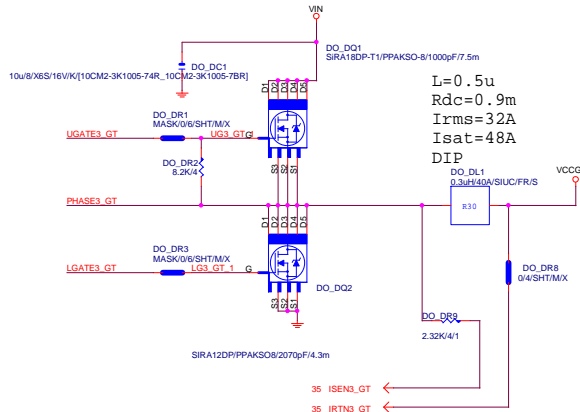
should be routed as differential pair,
7mil width, 8mil spacing, 20~30mil
others.



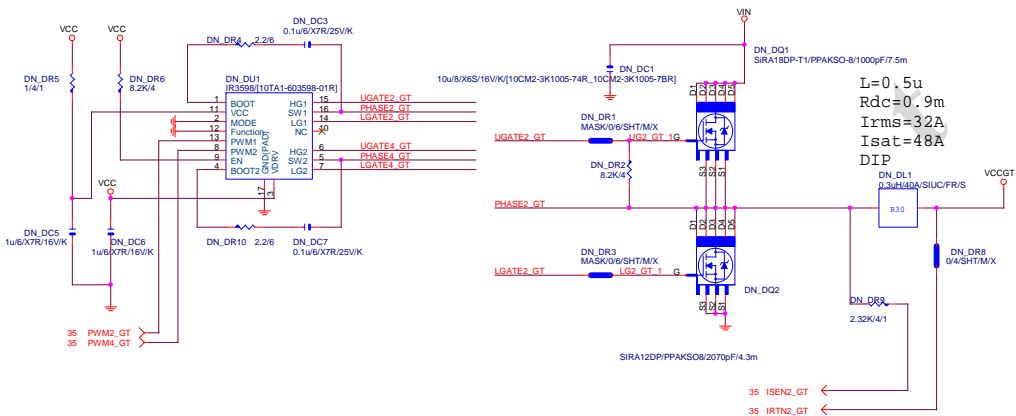
VCCGT-PHASE1



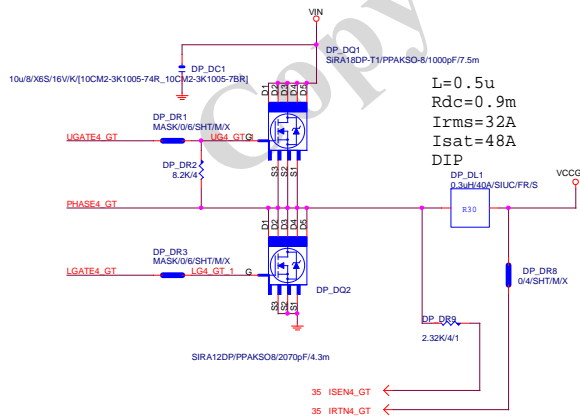
VCCGT-PHASE3



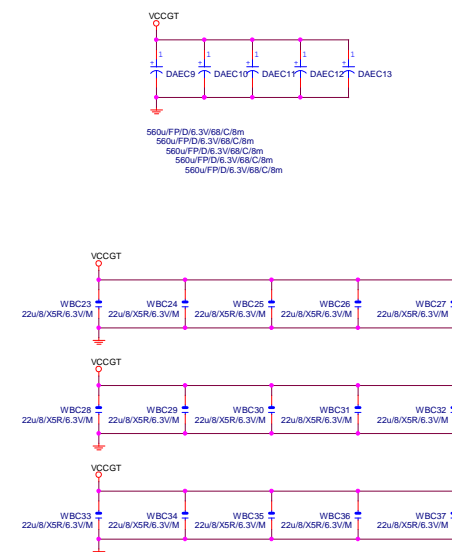
VCCGT-PHASE2



VCCGT-PHASE4



VCCGT CAP 560u*5PCS
22u*15PCS



39 VIO_ISEN1

39 VIO_IRTN1

DCC8

0.47u4/X5R/6.3V/K

DCR46

DCR45

301/4/1


DC I

DC I

DC I

[illegible]

should be routed as differential pair,
7mil width, 8mil spacing, 20~30mil
others.

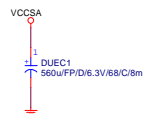

 VIO_EN DCR5 0/4/SHT/10/MX → VCCIO_EN 16
 Connect to IT8620


VCC3

DCR11
8.2k/4

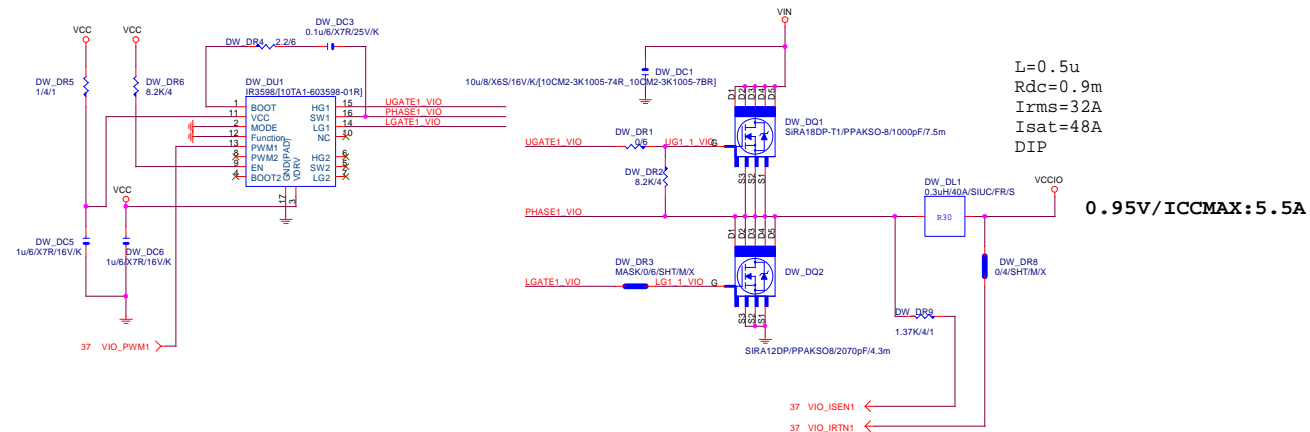
VIO_EN

REV:0.1



			
Title			
VCCSA MOS_IR3553			
Size	Document Number	Rev	
Custom	GA-Z170X-GAMING GT	1.01	
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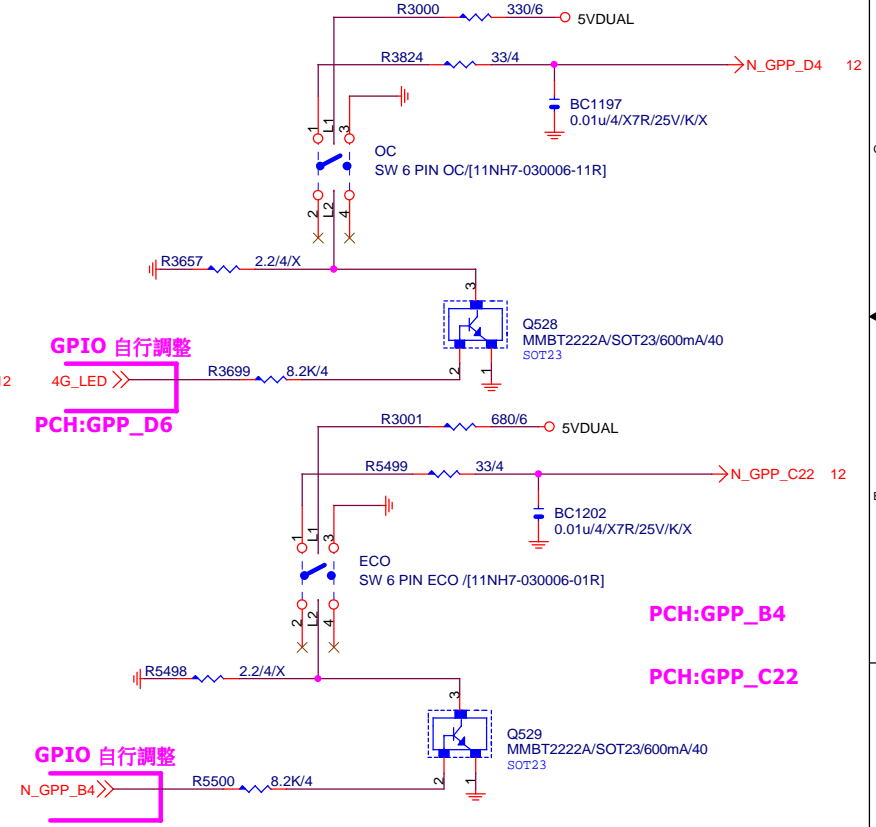
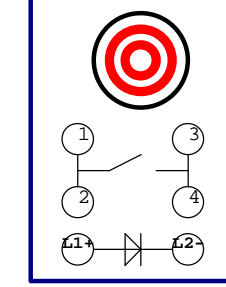
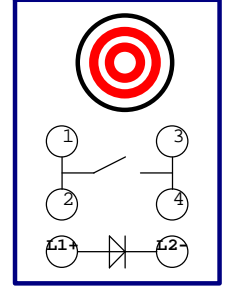
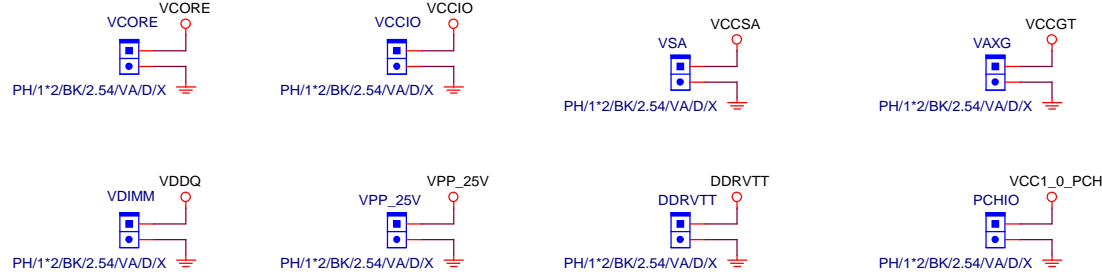
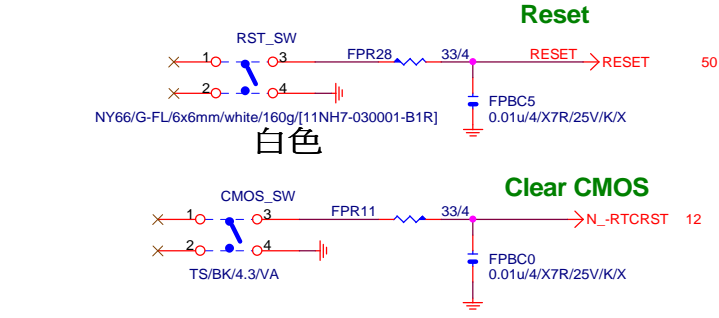
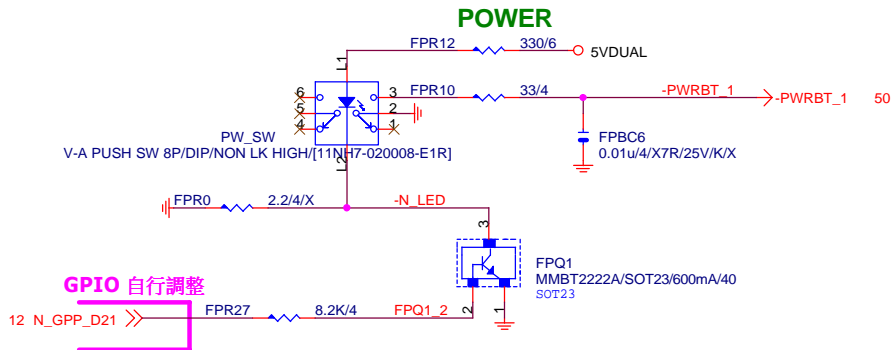
VCCIO REV:0.1



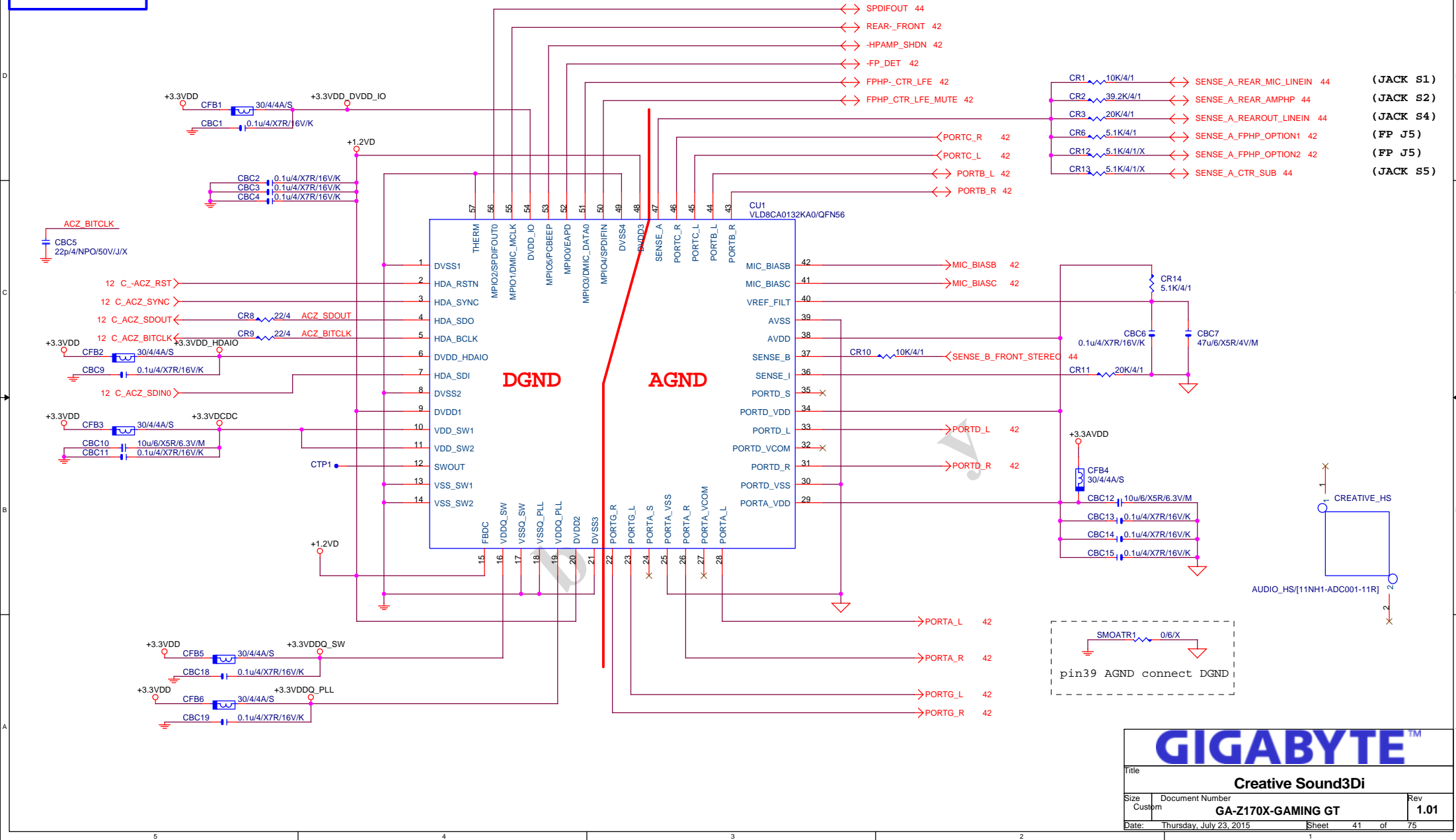
VCCIO CAP 560u*1PCS

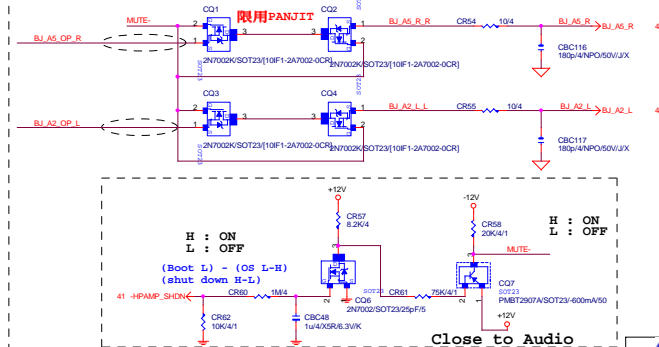
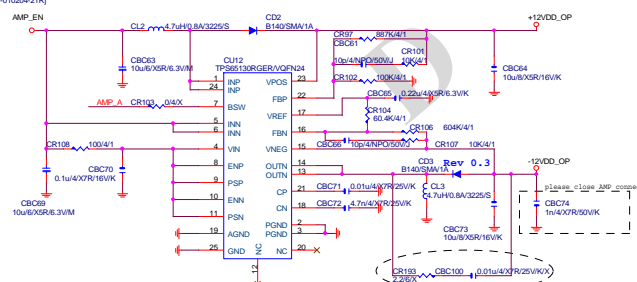
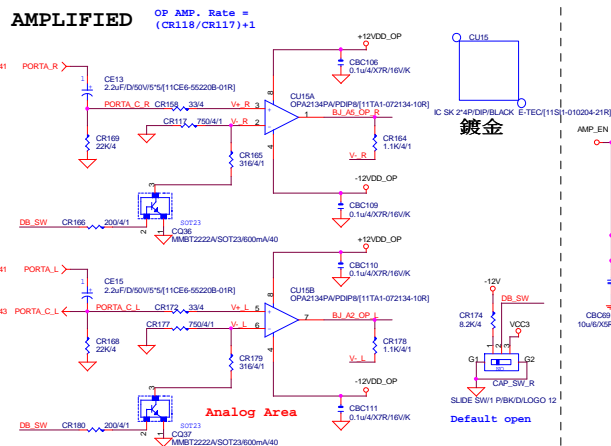
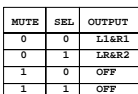
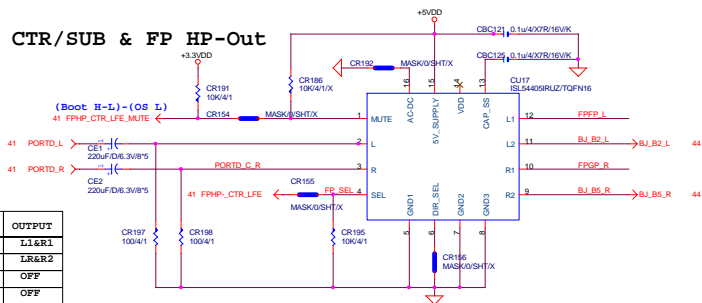
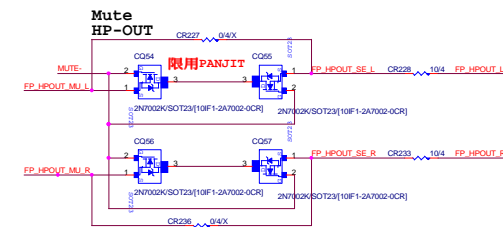
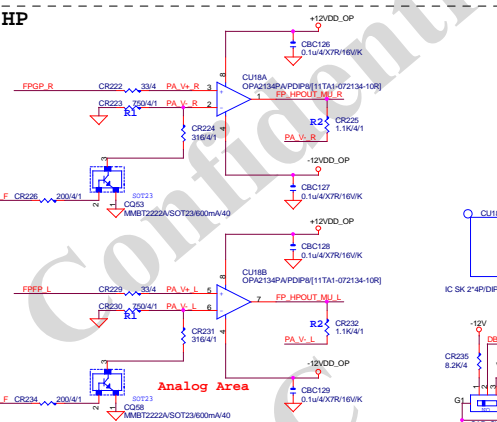
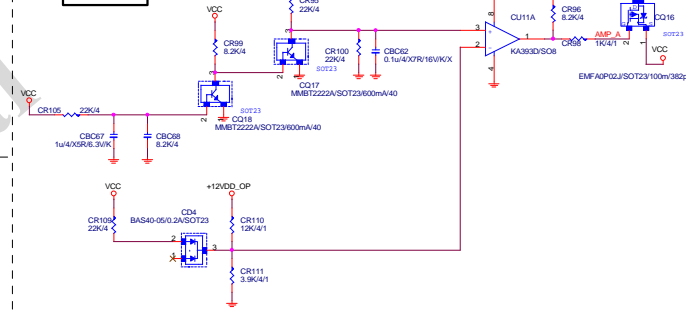
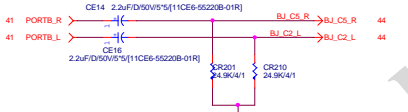
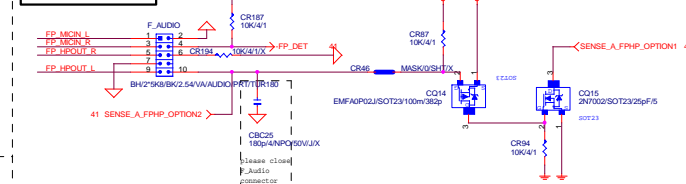
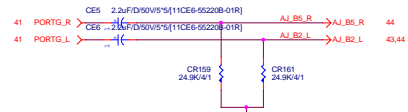
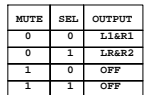


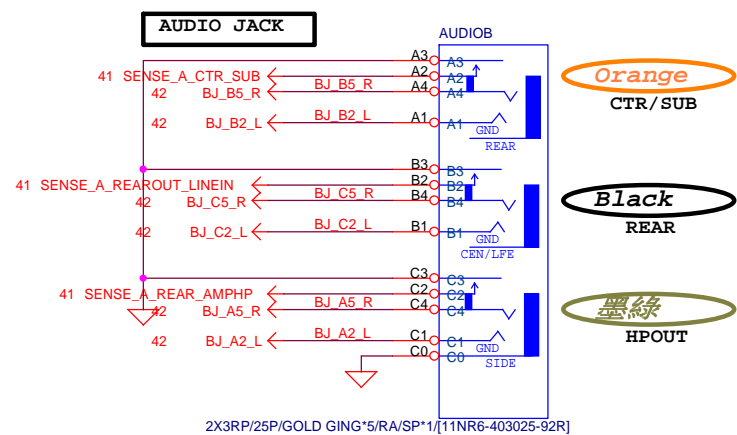
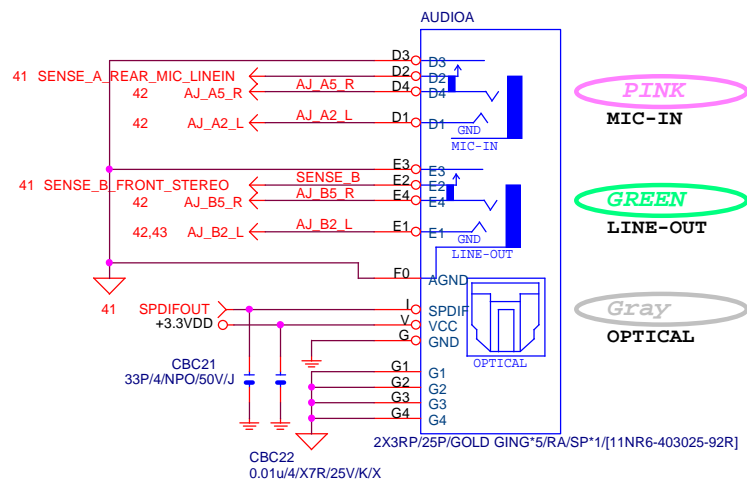
Gigabyte Technology			
VCCIO_MOS IR3553			
Size Custom	Document Number		Rev 1.01
GA-Z170X-GAMING GT			
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Gigabyte Technology			
Title			
OC BOTTOM			
Size	Document Number	Rev	
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**Gigabyte Technology**

Title

Creative Sound3Di ZxRSize
Custom

Document Number

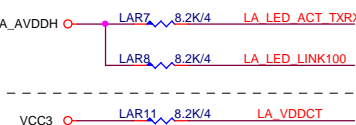
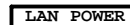
GA-Z170X-GAMING GT

Rev

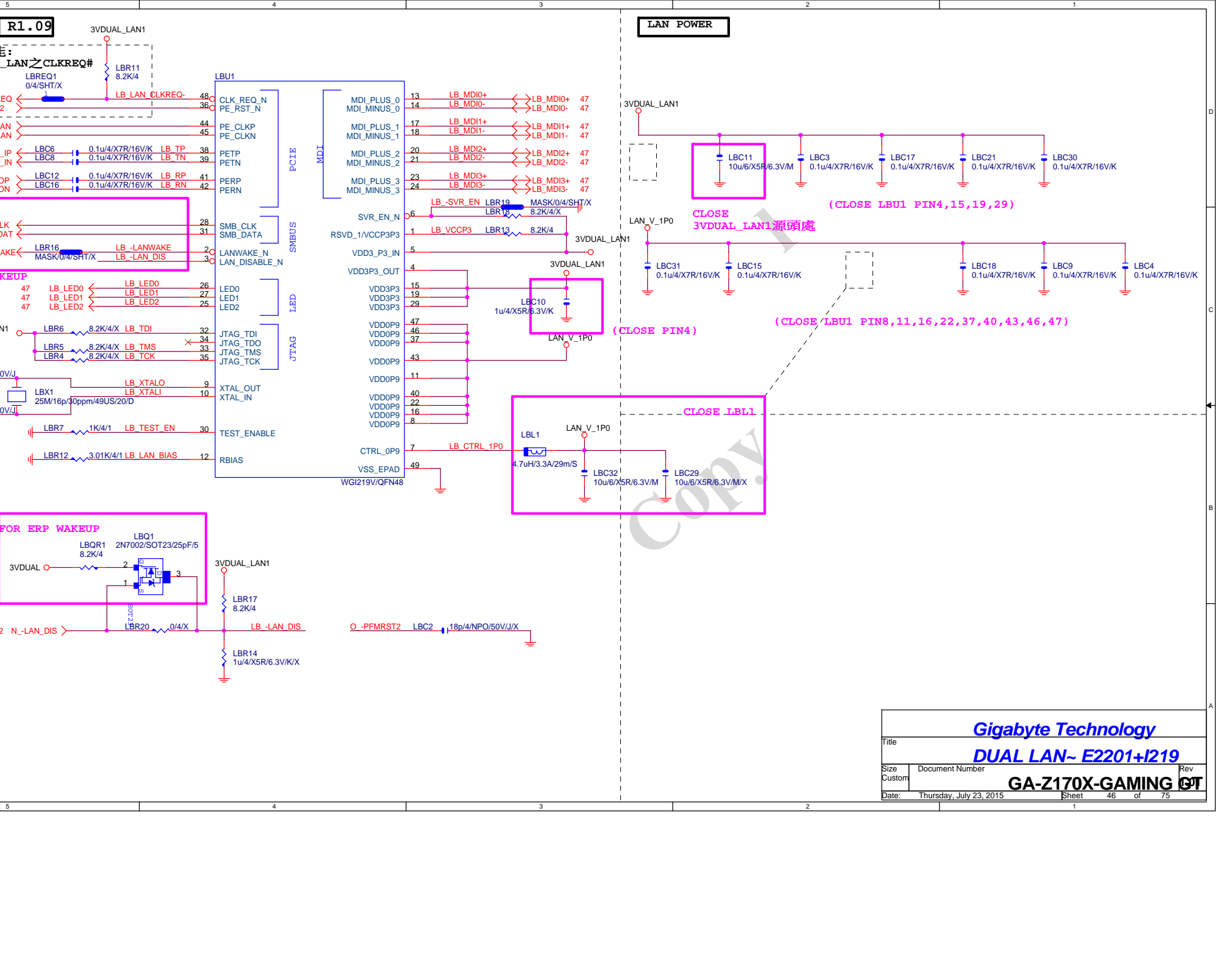
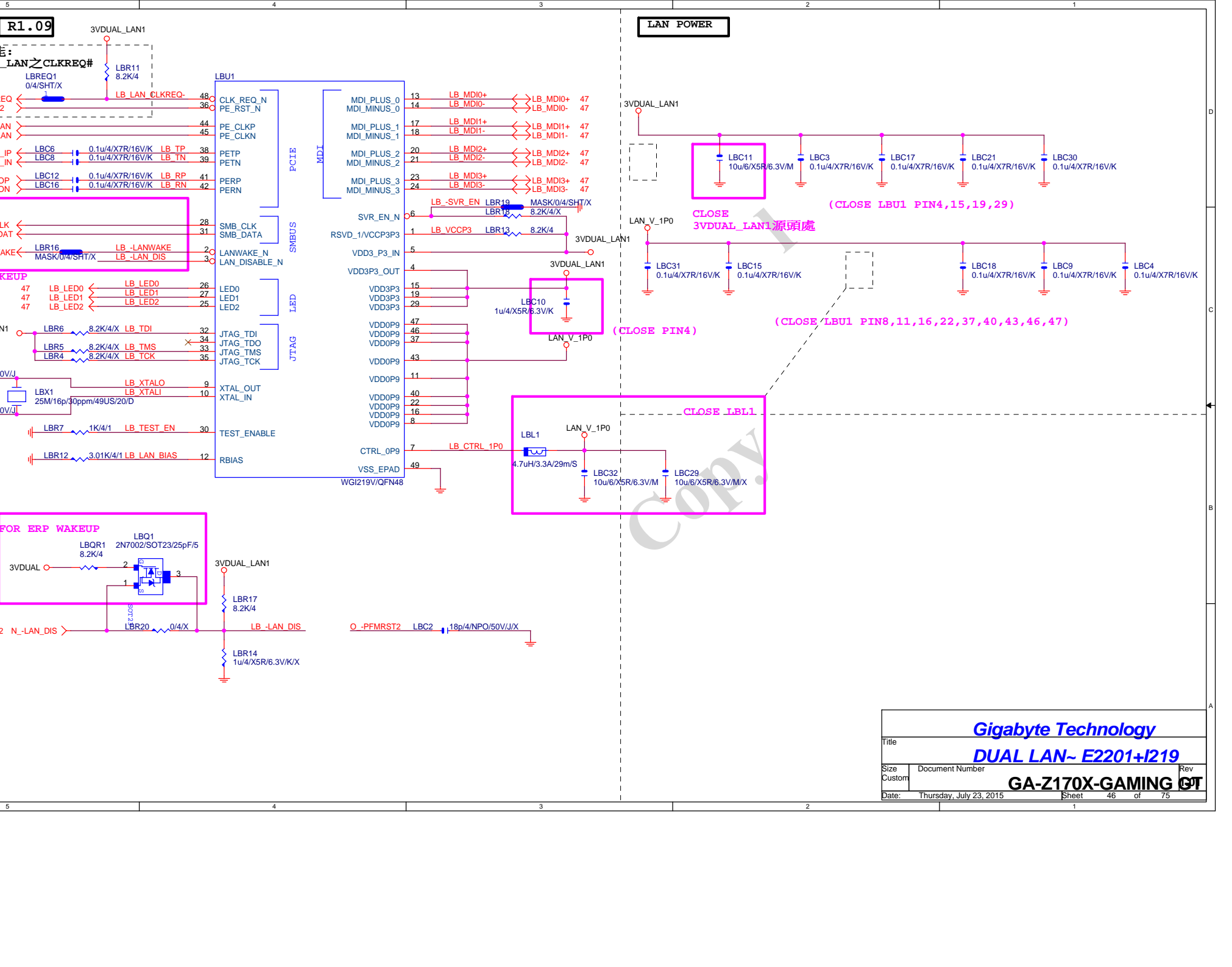
1.01

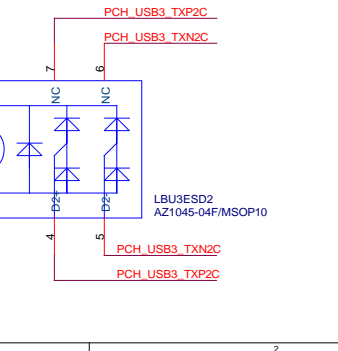
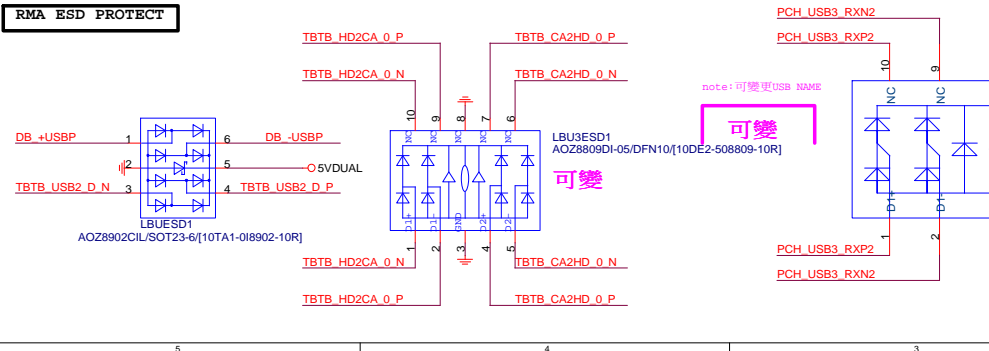
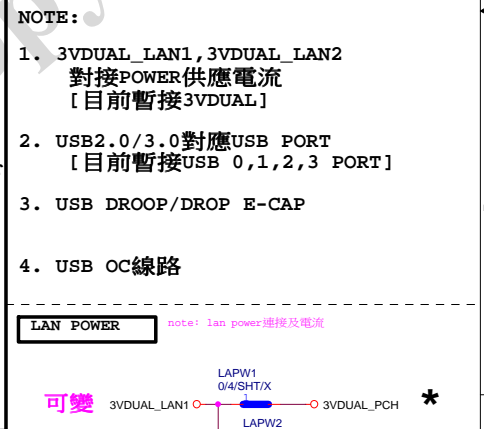
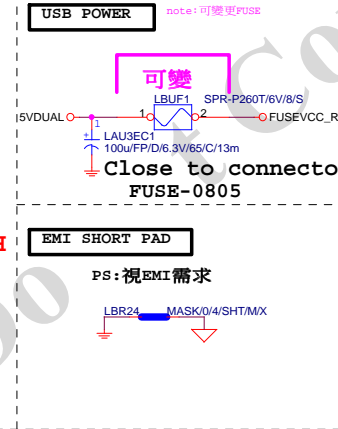
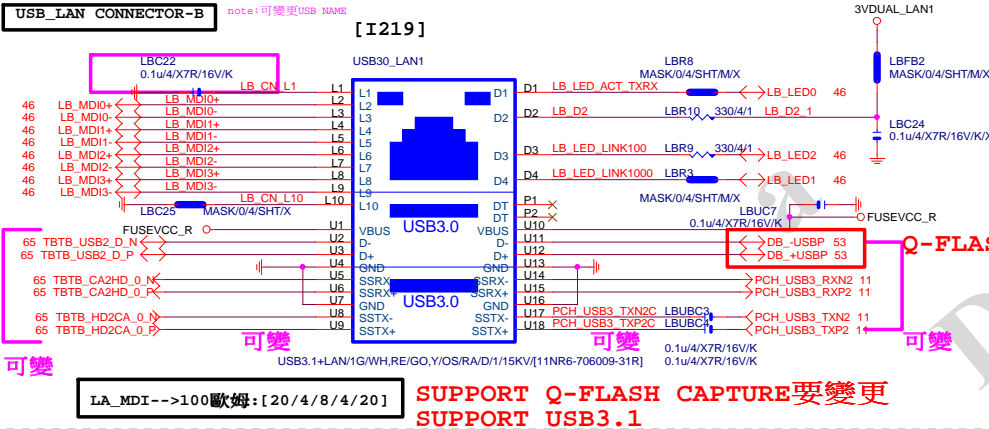
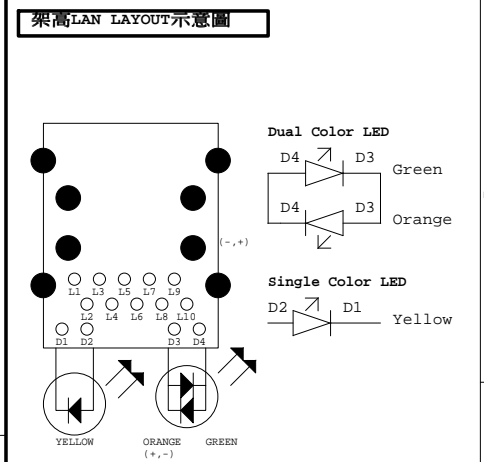
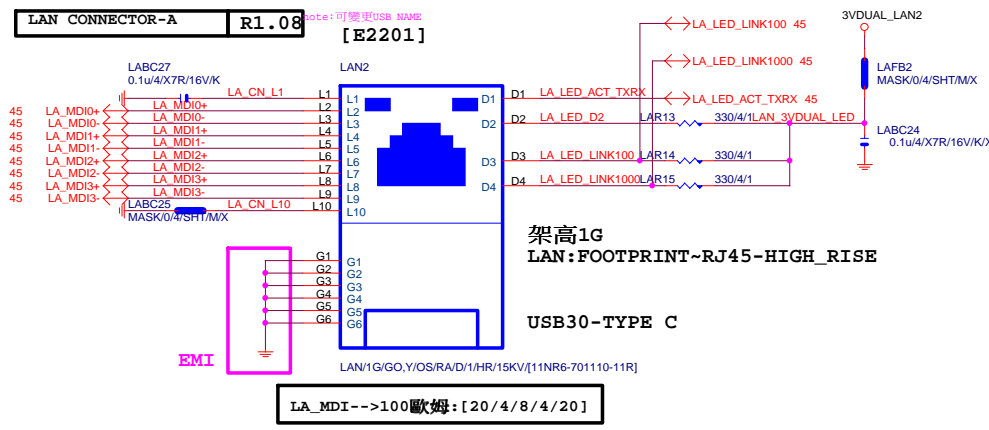
Date: Thursday, July 23, 2015

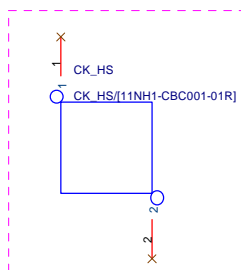
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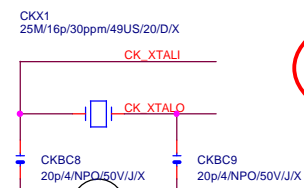
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Size	Document Number	Rev	
Custom	GA-Z170X-GAMING GT	1.01	
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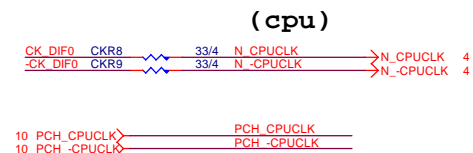
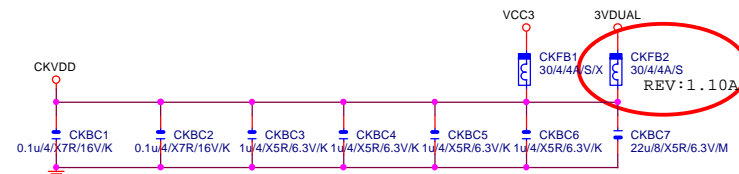
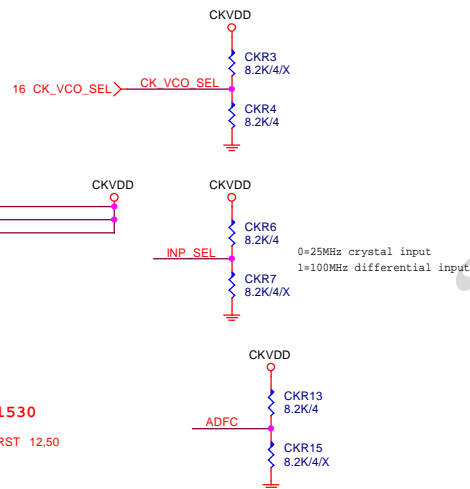
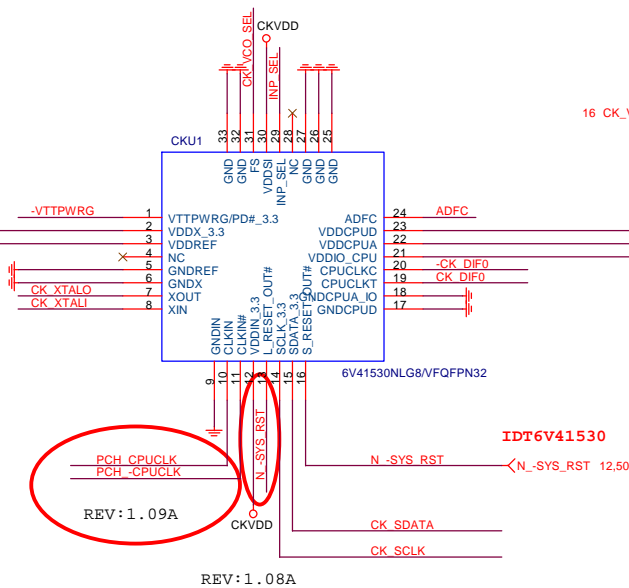




*可變，依需求上件不上件。

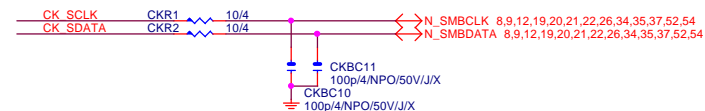
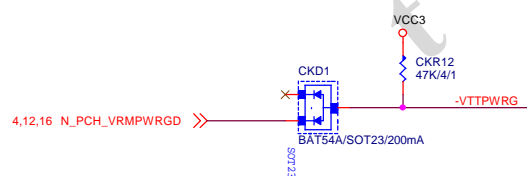


電容共用GND,降低JITTER

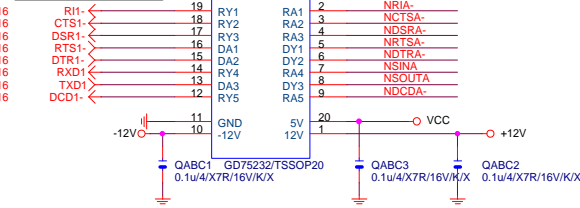


INP_SEL	Input
0	Crystal
1	CLK_INP/N

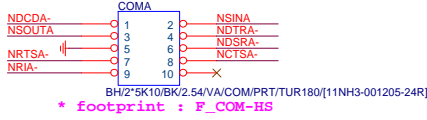
CK_VCO_SEL	VCO
0	400M
1	1200M



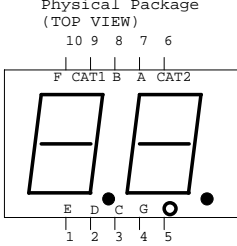
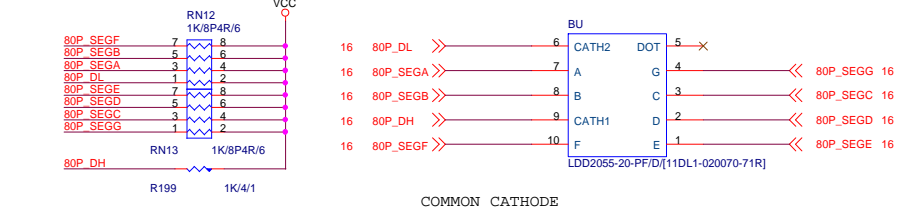
COM PORT



COMA

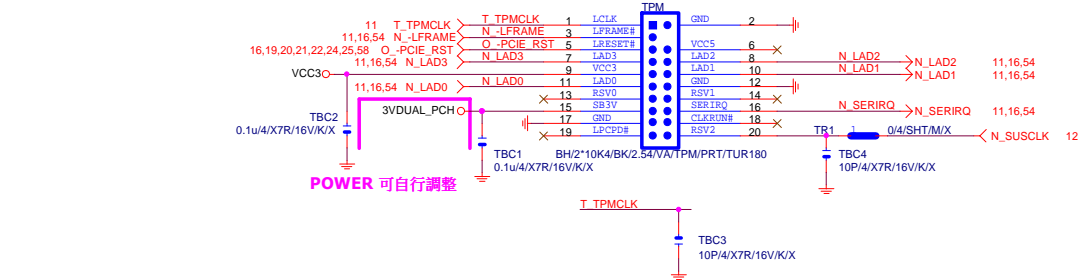


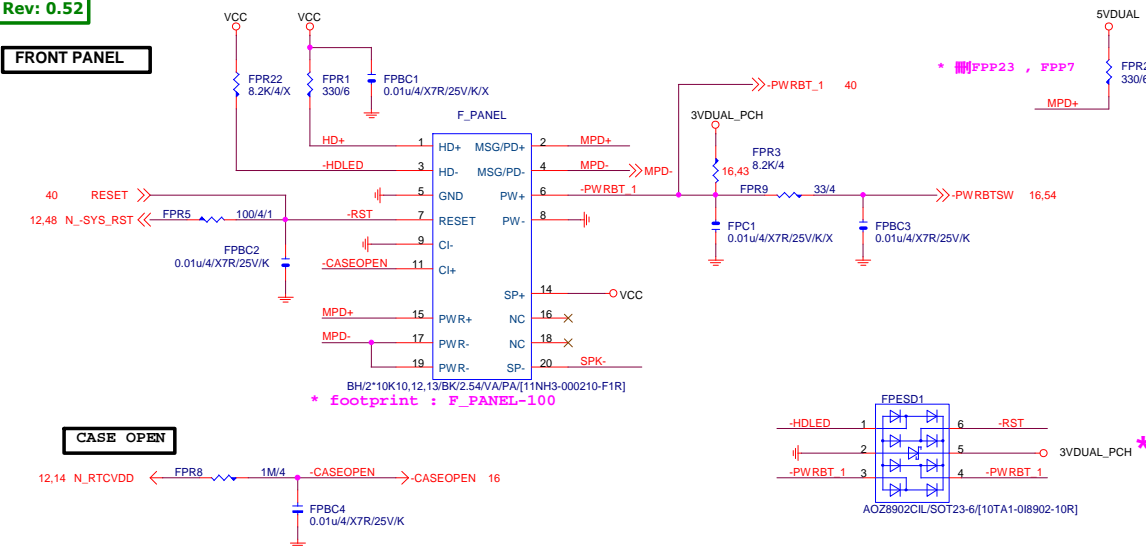
80 PORT



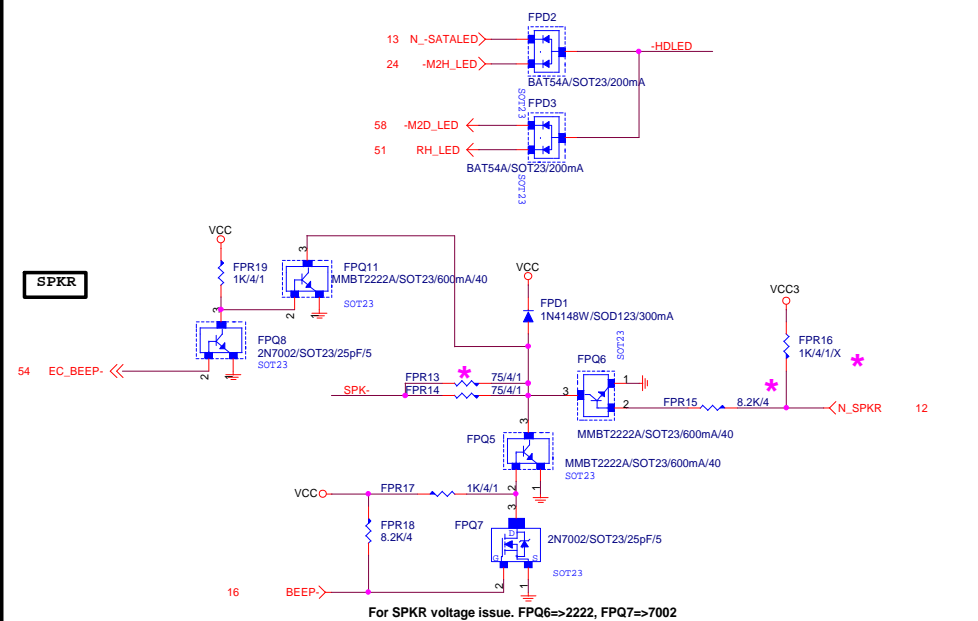
Thunderbolt

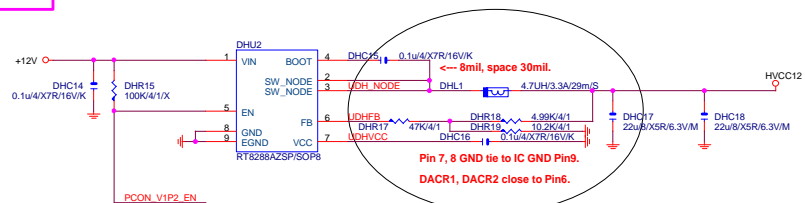
TPM CONNECT



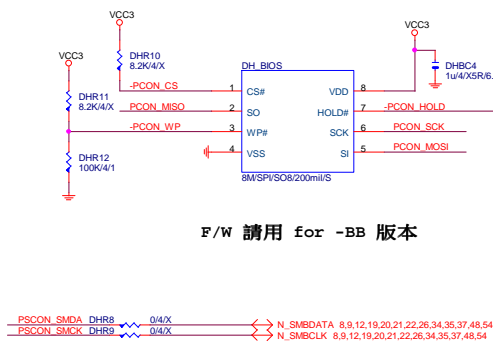
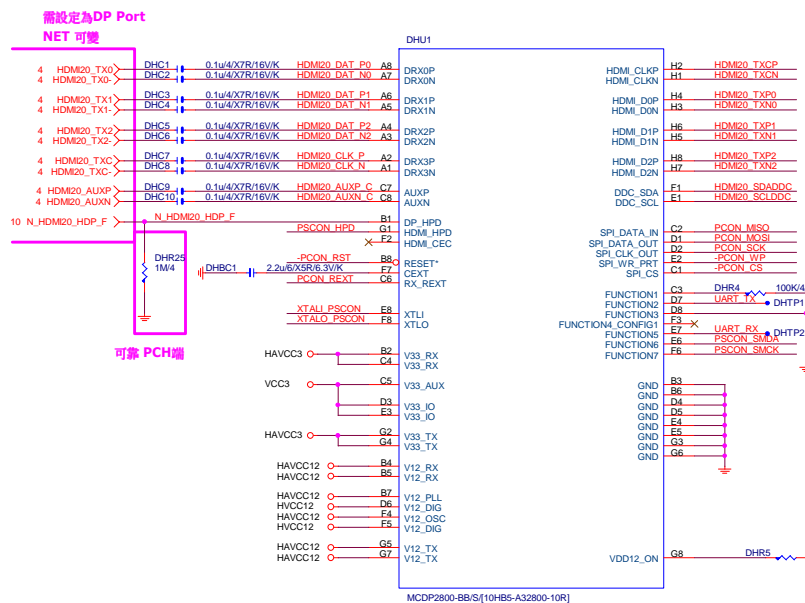
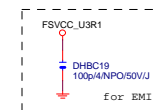
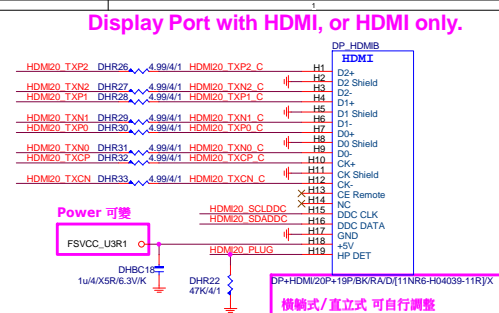
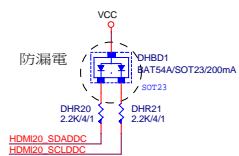


SATALED# signal open-collector, pull-up (8.2 k Ω to 10 k Ω) to Vcc3_3

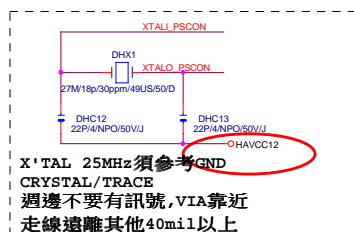
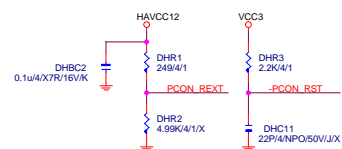
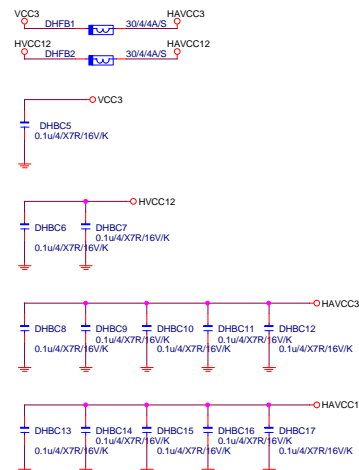




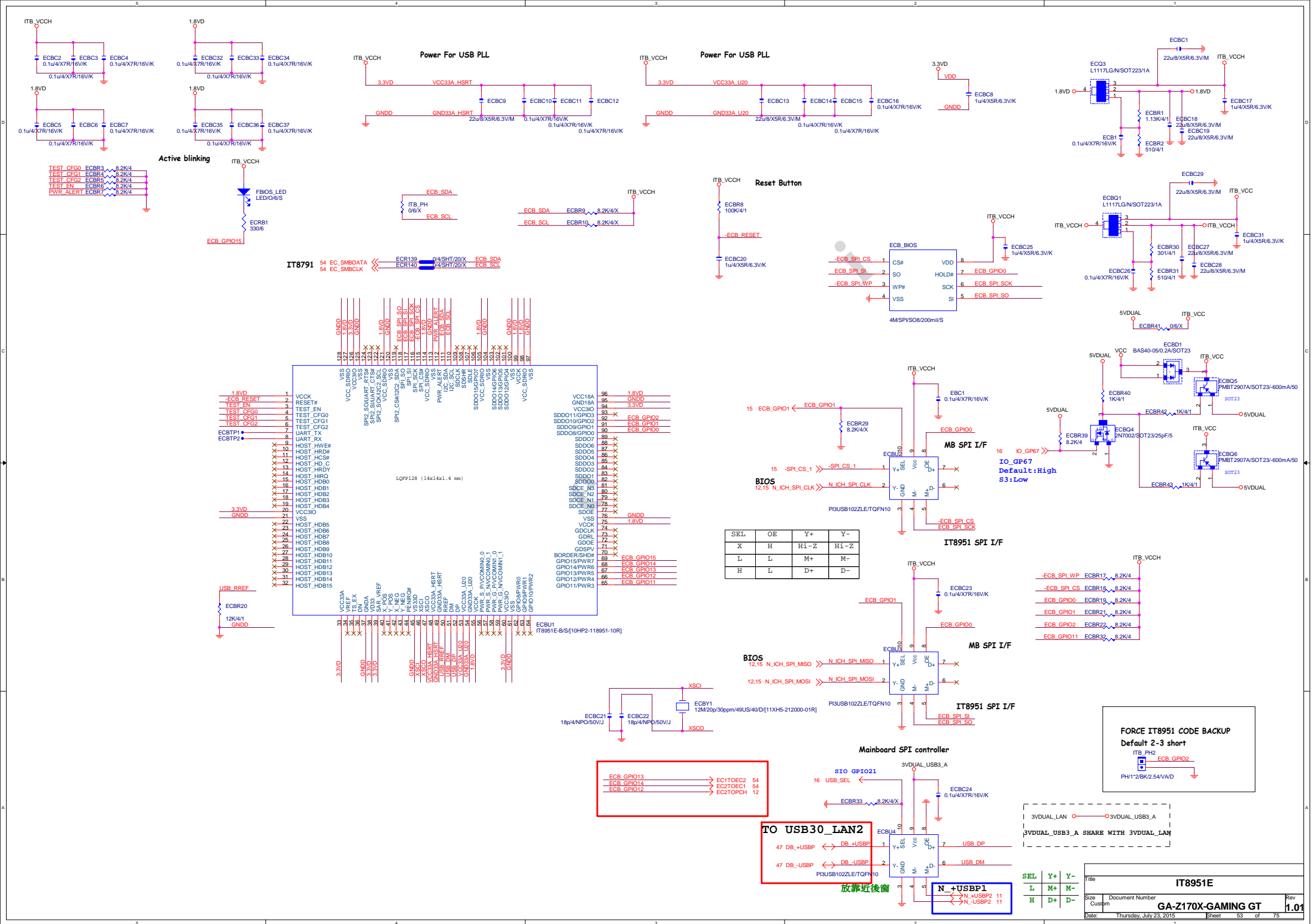
PCH端

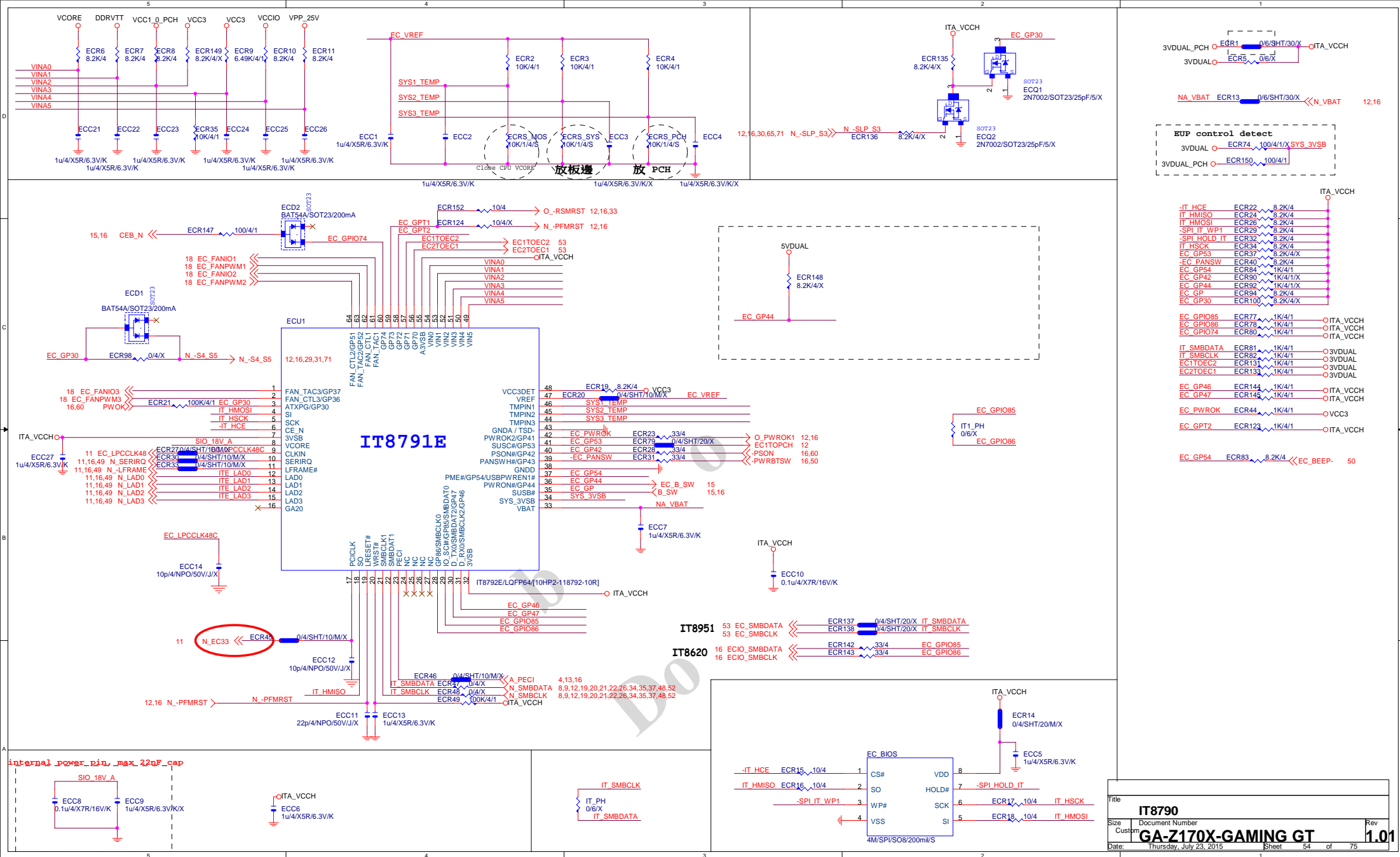


F/W 請用 for -BB 版本



X'TAL 25MHz 須參考 GND
CRYSTAL/TRACE
週邊不要有訊號, VIA 靠近
走線遠離其他 40mil 以上

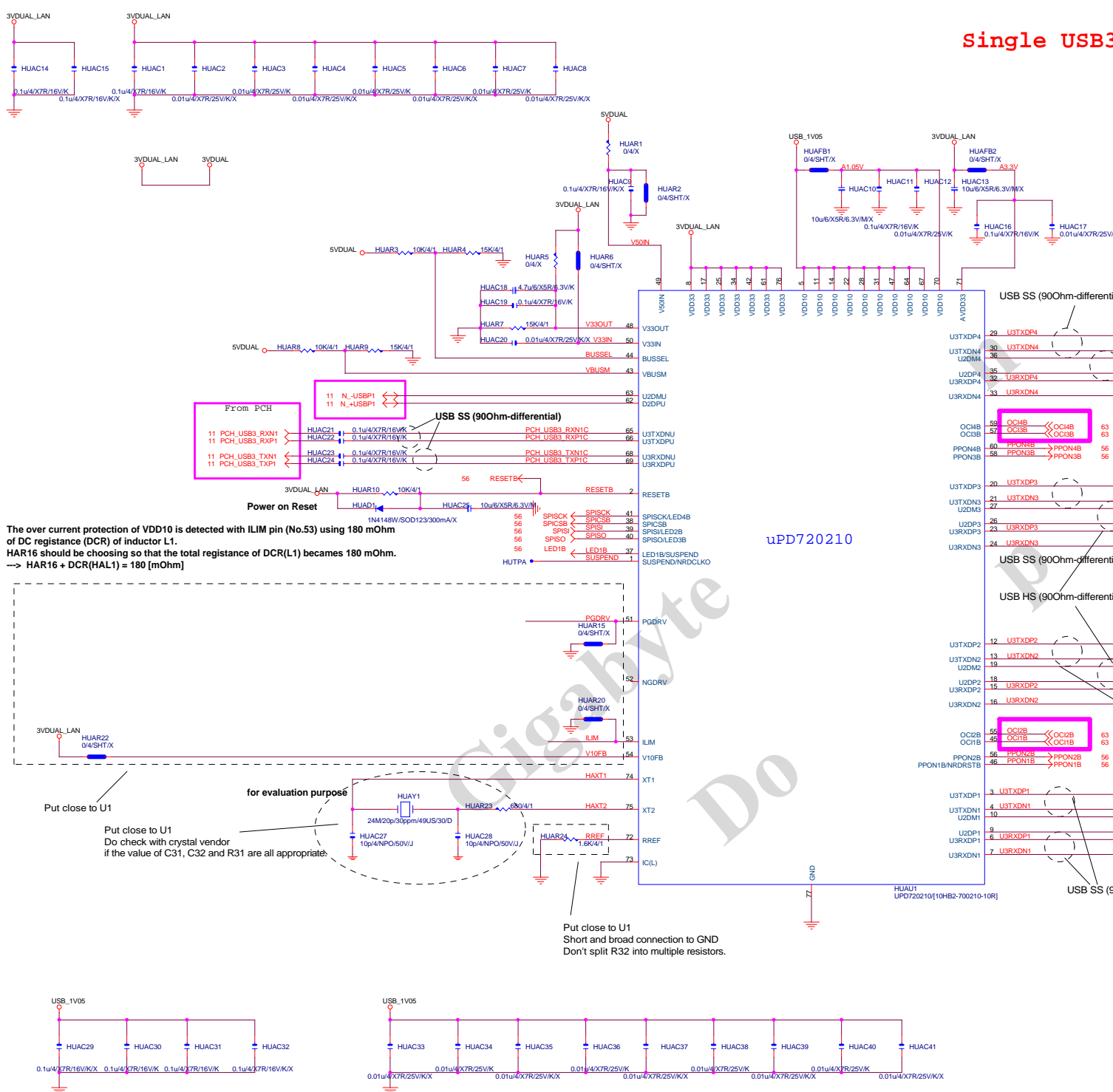




Single USB HUB used

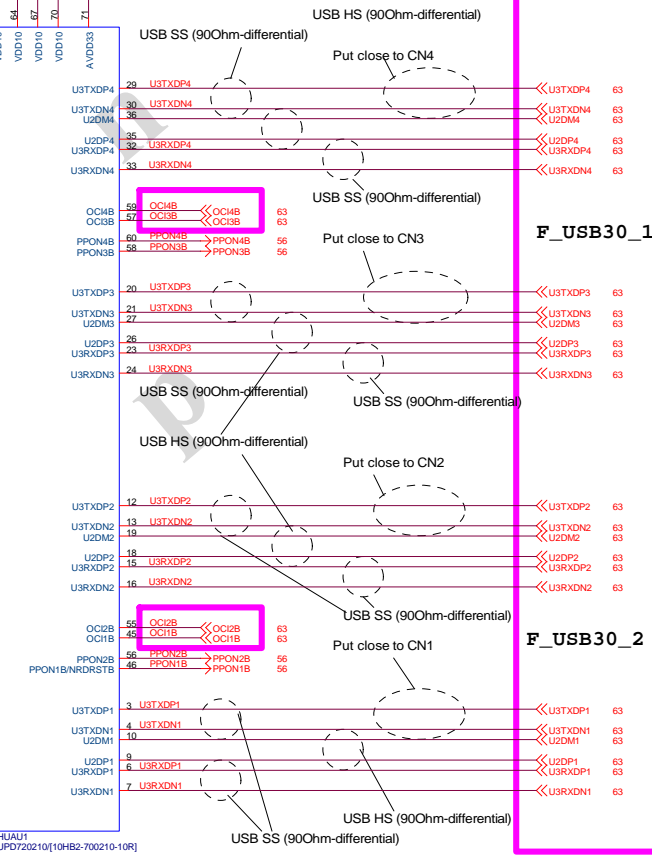
Rev 0.3

Link to Connectors and OC circuits



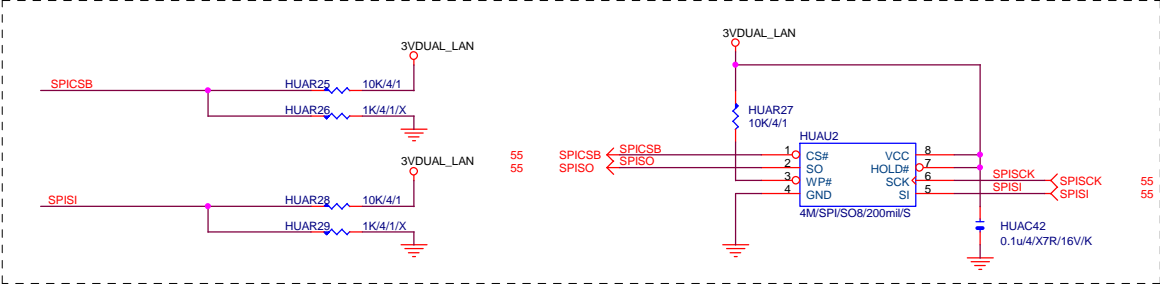
The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]

uPD720210

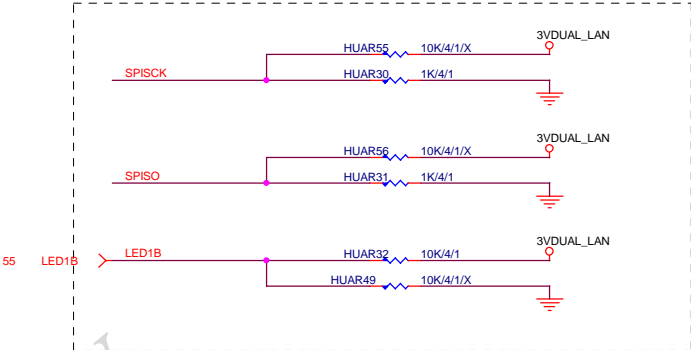


Single USB3 HUB used

External SPI ROM ; SPI ROM attached mode

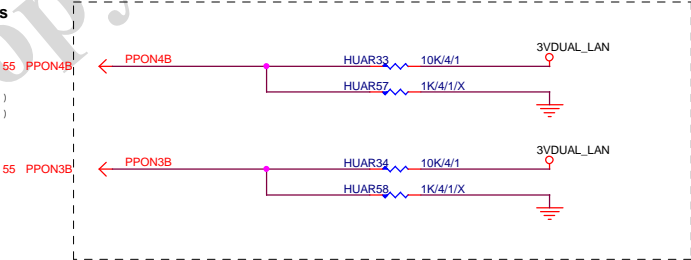


Battery Charging

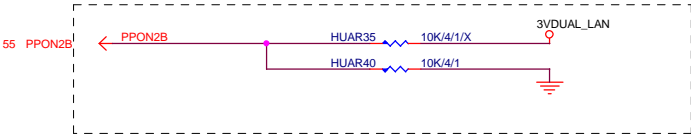


Number of Ports ; 4Ports mode

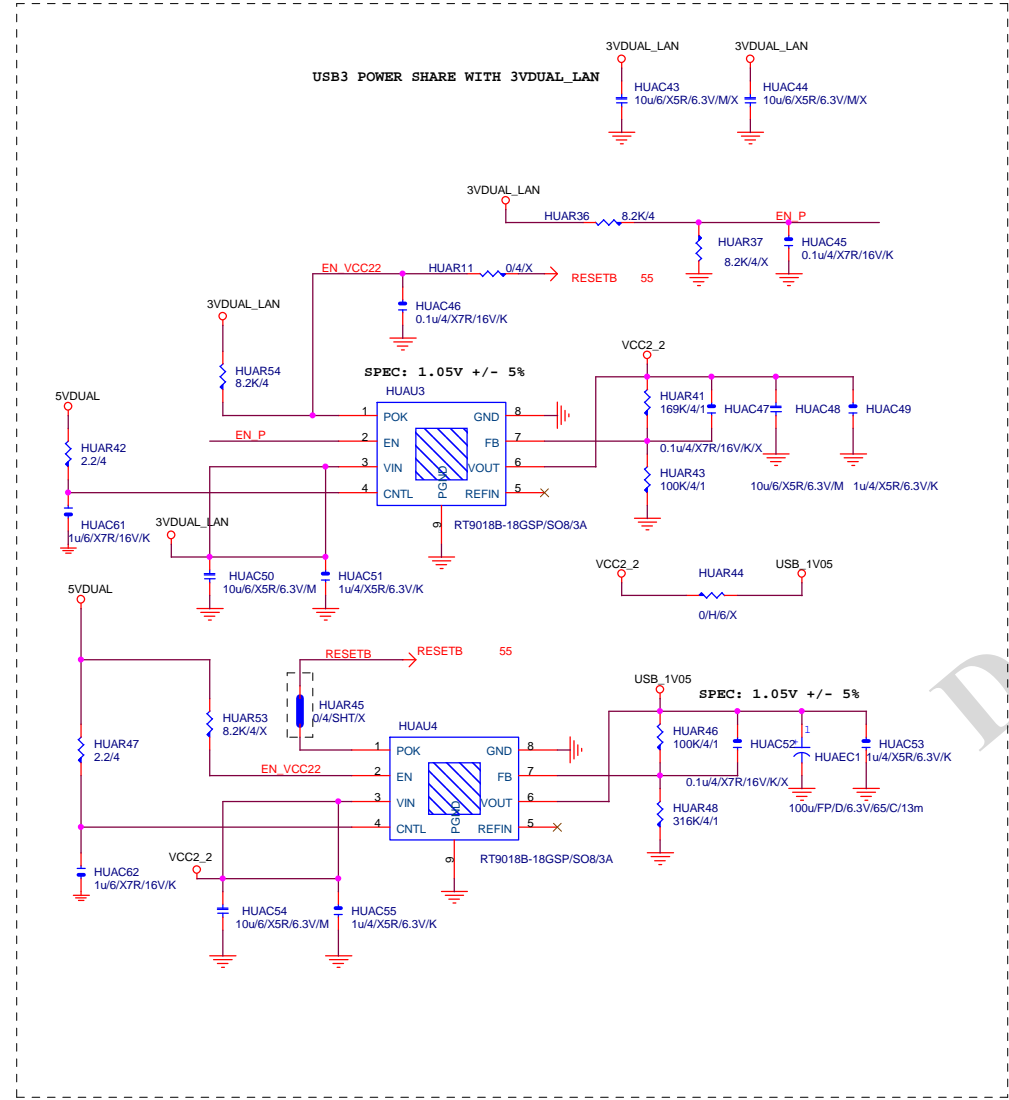
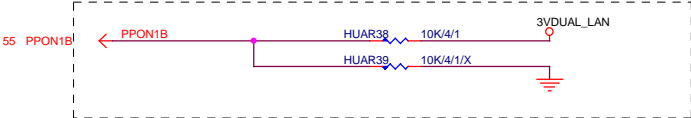
PPON3B / PPN4B : H / H (4 port)
PPON3B / PPN4B : L / L (2 port)



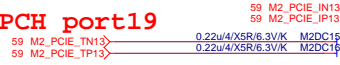
#5 VBUS Power Control ; Individual mode



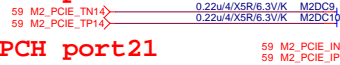
PPON1B Pin Function ; Port1 PPONB mode



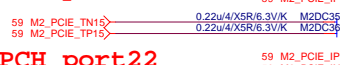
M.2 Lane2 from PCH port19



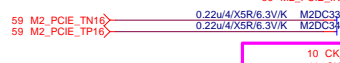
M.2 Lane2 from PCH port20



M.2 Lane3 from PCH port21

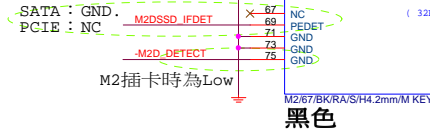
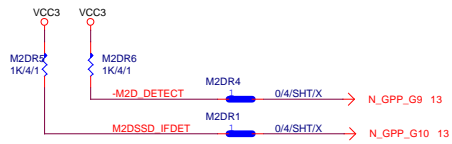


M.2 Lane4 from PCH port22



需與M2_-CLKREQ對應

支援SATA and M.2 function



黑色

M.2-SATA(S3)+SATA S0&S1&S2

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	H (SATA)	GPP_C21	H

M.2-SATA(S3)+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	L (S.E.)	GPP_C21	H

M.2X4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	N/A	GPP_C21	H

M.2X2+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	L	GPP_C21	H

M.2X2+SATA S0&S1

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

M.2沒插卡+SATA S0~S3

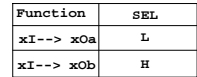
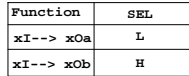
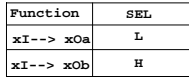
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	H	GPP_C21	L

M.2沒插卡+S.E.C&S.E.D

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	L	GPP_C21	L

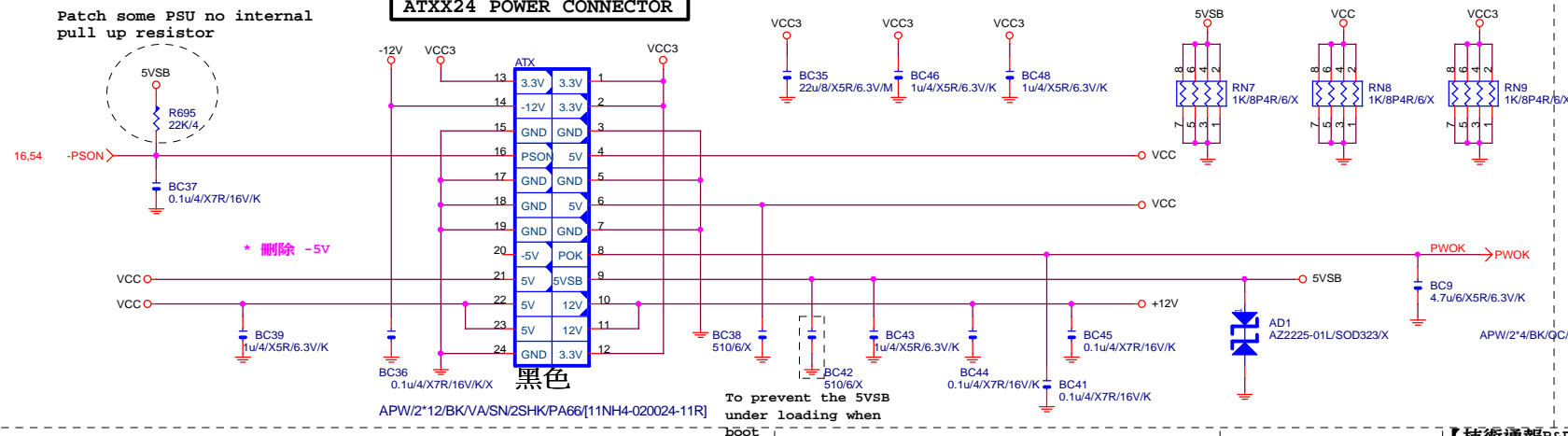
M.2 有插卡 / 沒插卡?	M.2插何種卡? GPP_G10	SATA Express 插何種硬碟? GPP_E0/E1/E2/F0	IO19 (S0)	IO20 (S1)	IO21 (S2)	IO22 (S3)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (S0)	SATA (S1)	SATA (S2)	SATA (S3)
	PCIE Mode (Hi)	SATA Express (Low)	SATA Express (For S.E.0)	PCIEx4 (For M.2)	PCIEx4 (For M.2)	SATA (For M.2)
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	SATA (S0)	SATA (S1)	SATA (S2)	SATA (S3)
		SATA Express (Low)	SATA Express (For S.E.0)	SATA Express (For S.E.1)	SATA Express (For S.E.1)	

GIGABYTE Technology			
Title	M.2 X4		
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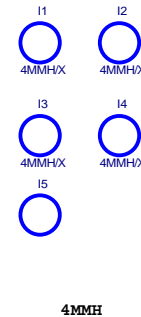
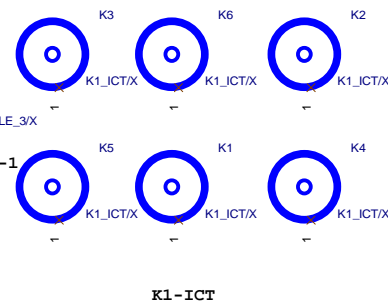
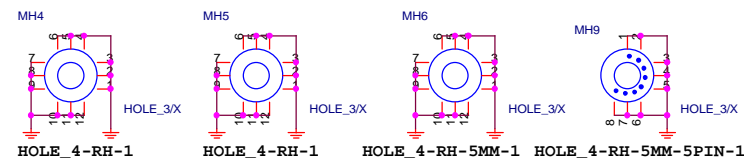
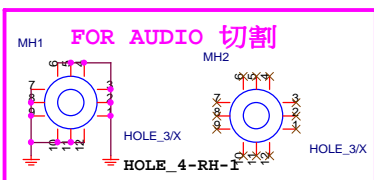
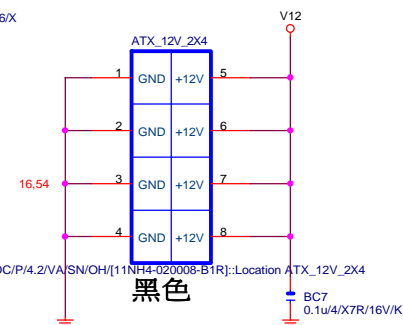


Patch some PSU no internal pull up resistor

ATXX24 POWER CONNECTOR

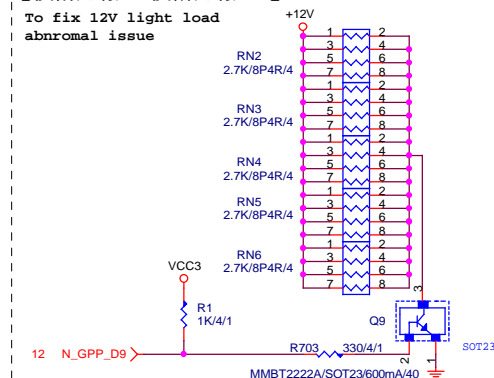


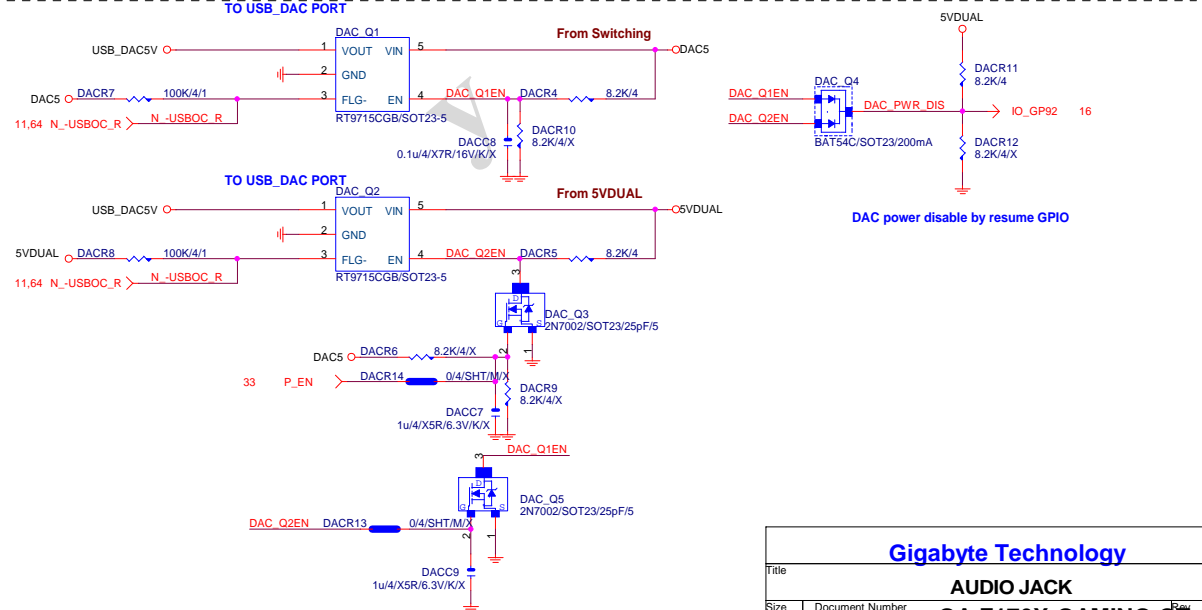
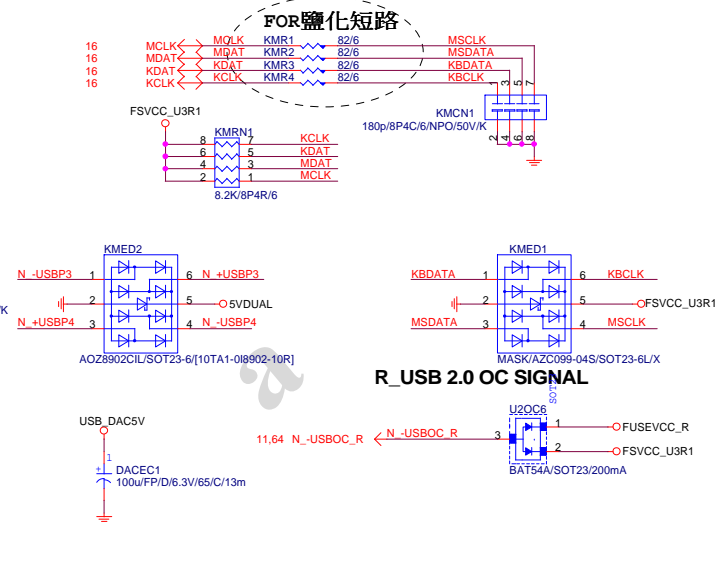
ATXX4 POWER CONNECTOR



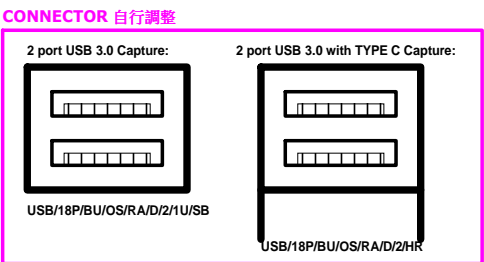
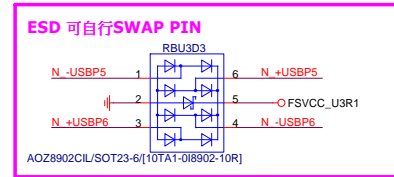
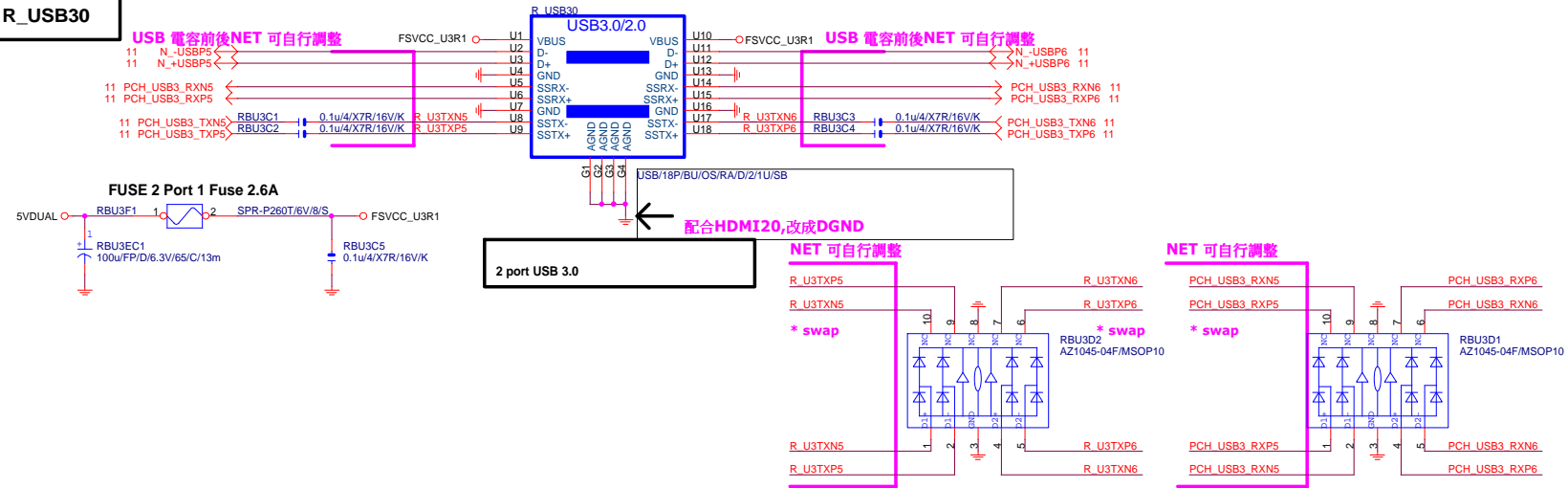
【技術通報R&D技術通報153】

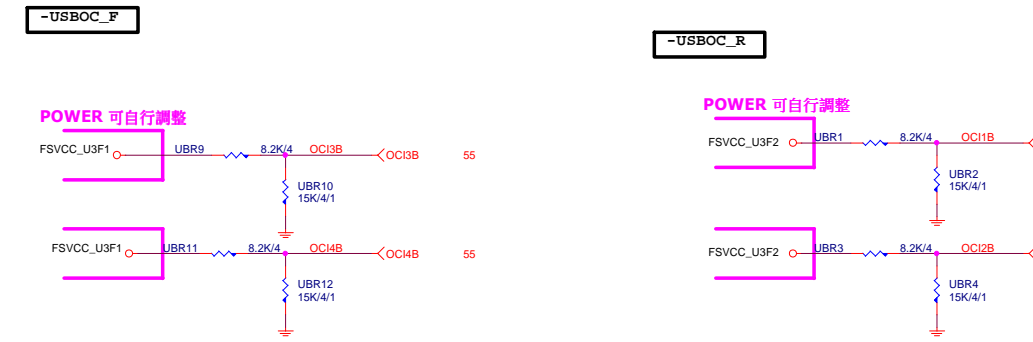
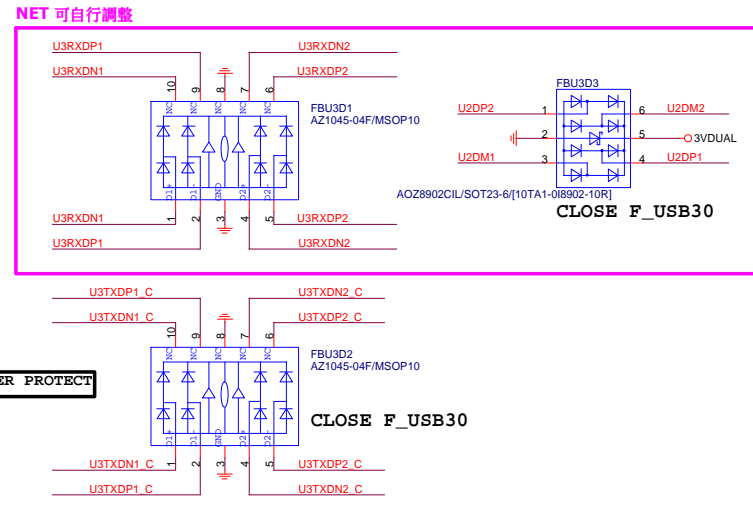
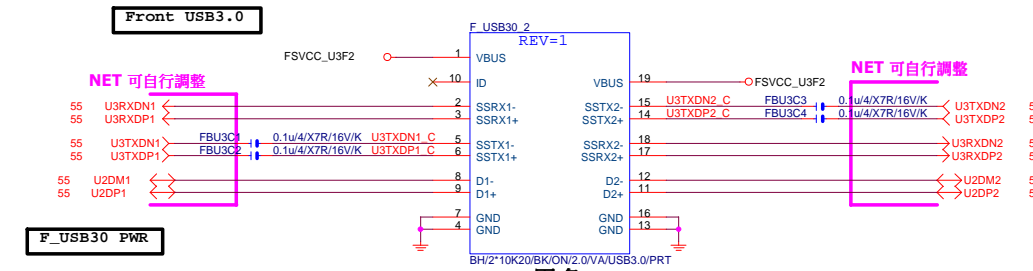
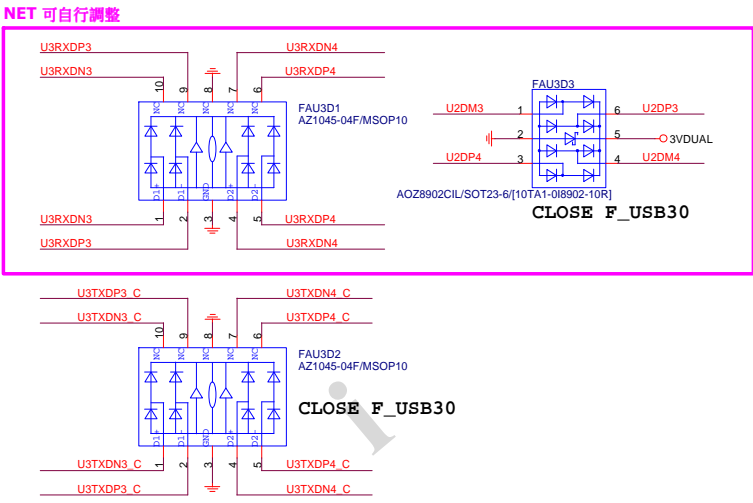
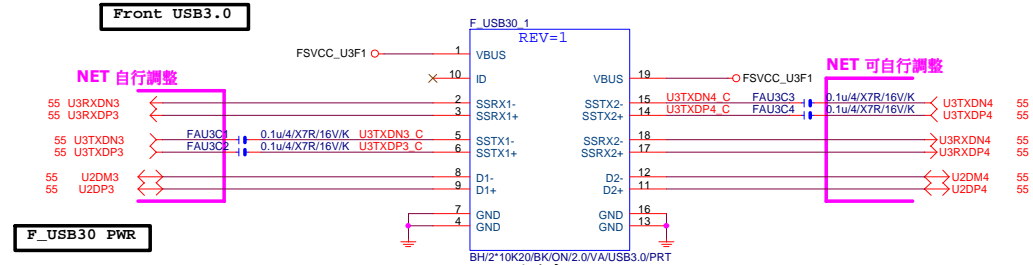
To fix 12V light load abnormal issue





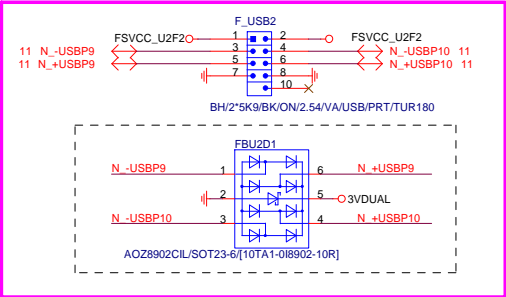
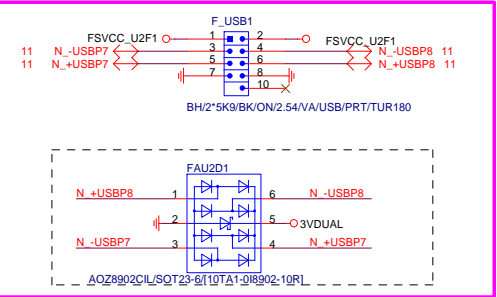
R_USB30





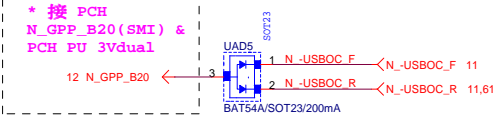
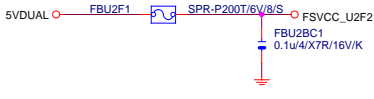
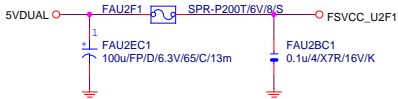
NET 可變

NET 可變

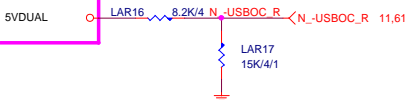
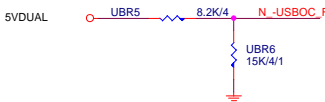


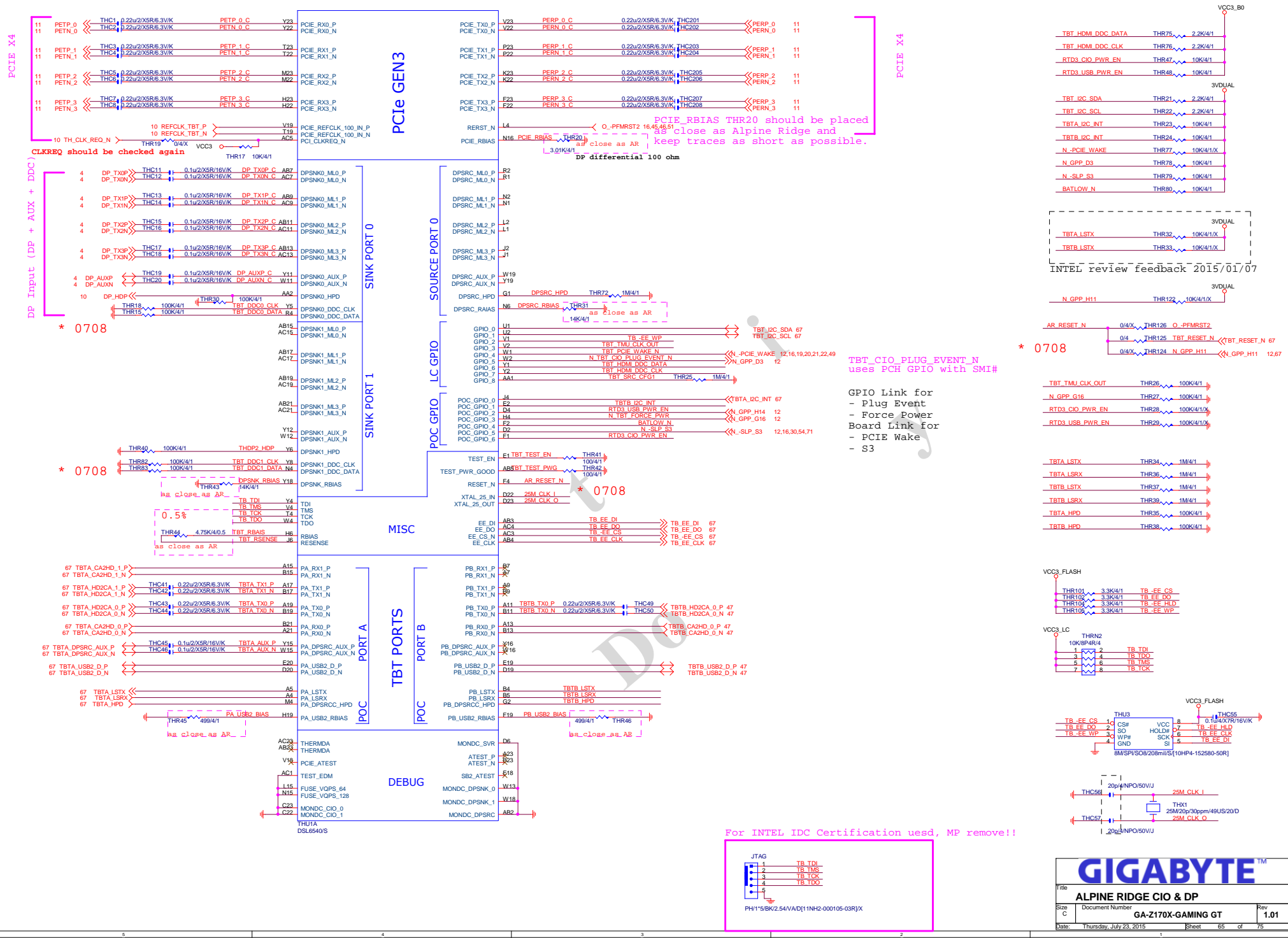
Close to connector
FUSE 2 Port 1 Fuse 2A

Close to connector
FUSE 2 Port 1 Fuse 2A



F_USB 2.0 OC SIGNAL





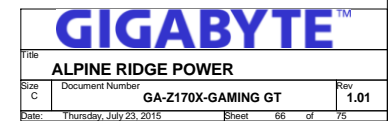
PCIE_RBIAS THR20 should be placed
close as Alpine Ridge and
keep traces as short as possible.

TBT_CIO_PLUGIN_N
uses PCH GPIO with SMI#

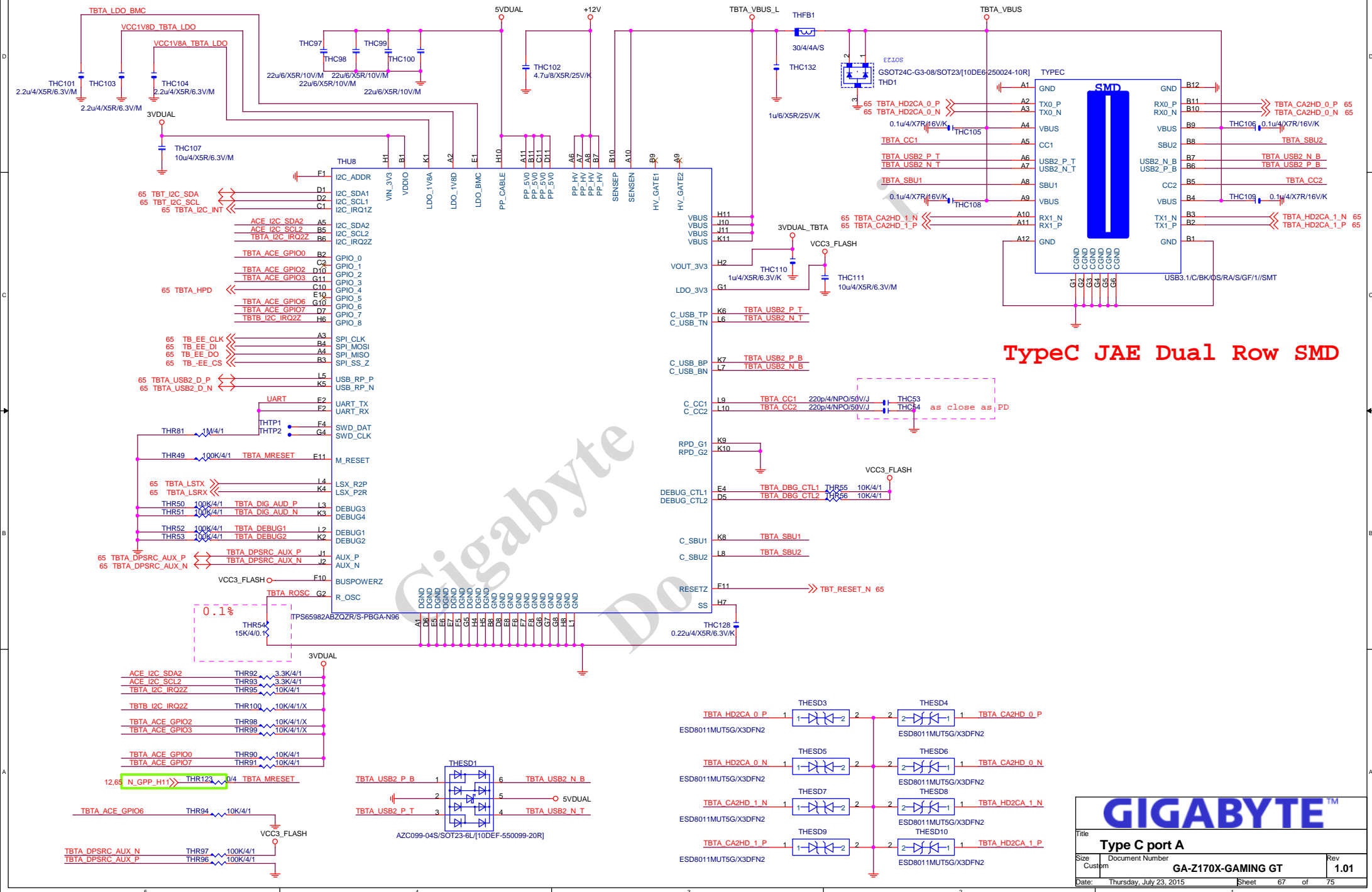
GPIO Link for
- Plug Event
- Force Power
Board Link for
- PCIE Wake
- S3

For INTEL IDC Certification used, MP remove!!

Base on INTEL AR reference SCH 1.0 (2015/05/11)



Base on INTEL AR reference SCH 1.01 (2015/05/13)



D

D

C


C

B


B

A

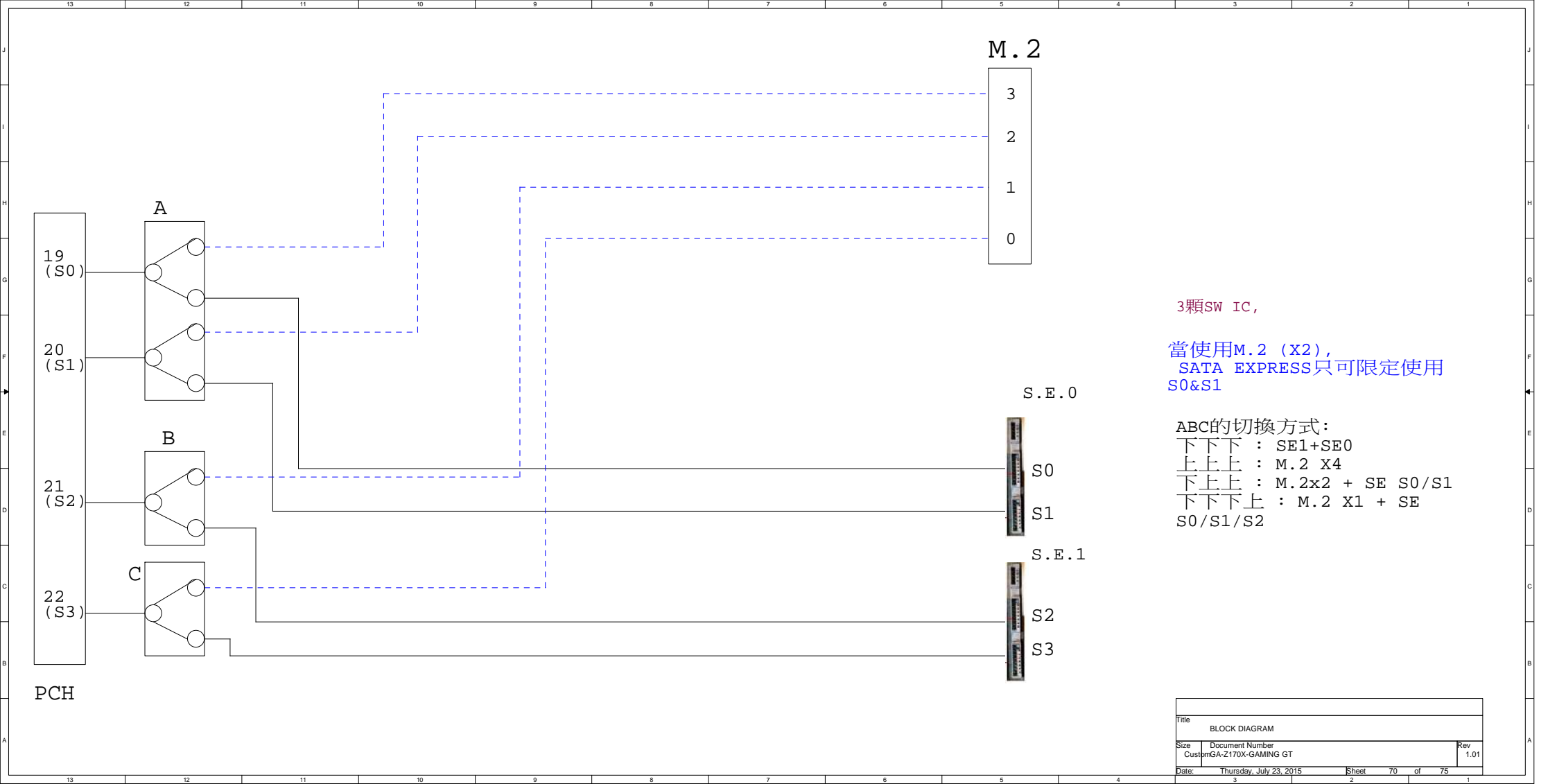
A



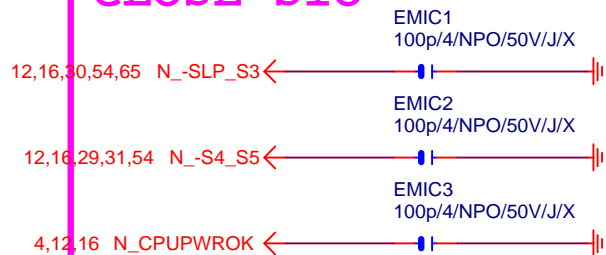
Title			
Type C port A			
Size	Document Number		Rev
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Date:	Thursday, July 23, 2015	Sheet 68 of 75	



Title			
TBT _ HDMI 2.0			
Size	Document Number		Rev
Custom	GA-Z170X-GAMING GT		1.01
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CLOSE SIO



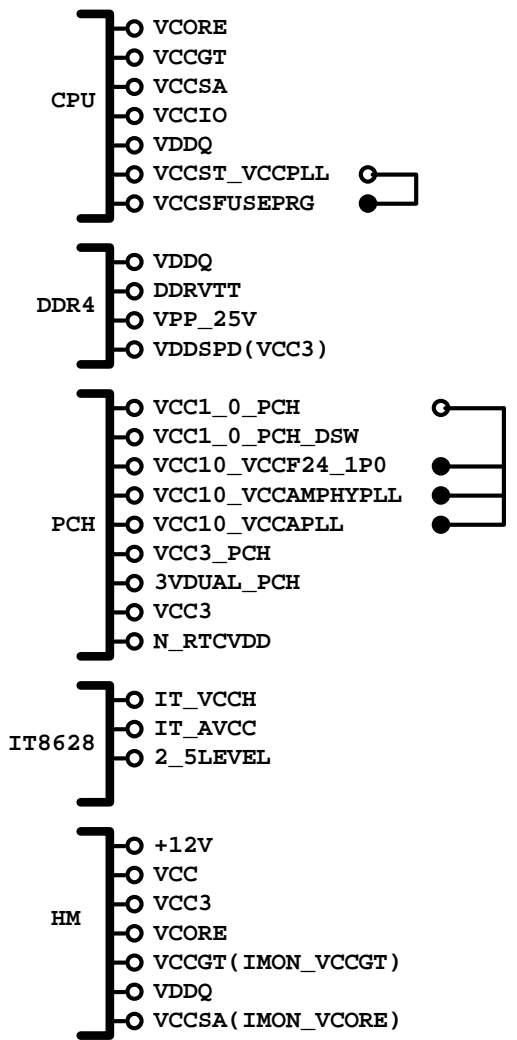
CLOSE PCH



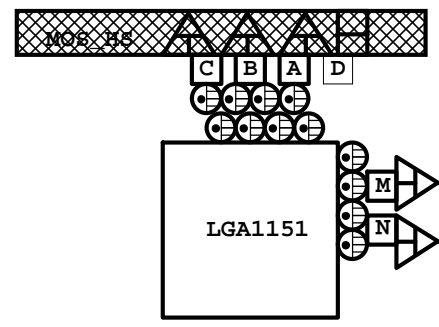
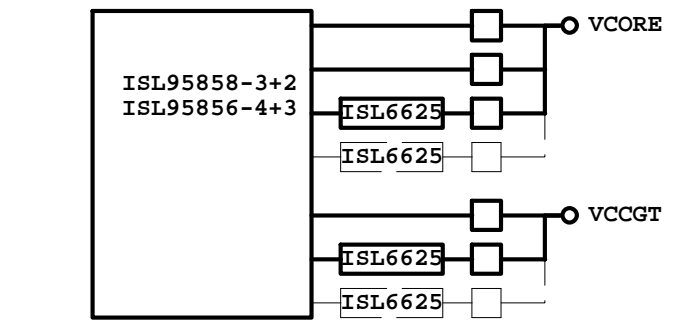
GIGABYTE™

Title		
EMI/ESD		
Size A	Document Number GA-Z170X-GAMING GT	Rev 1.01
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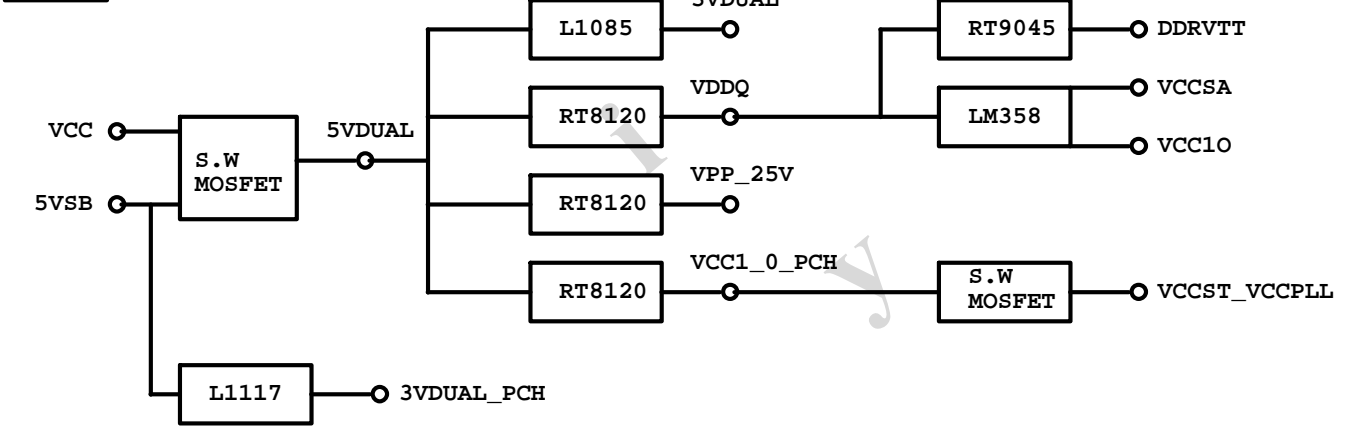
POWER BLOCK MAP



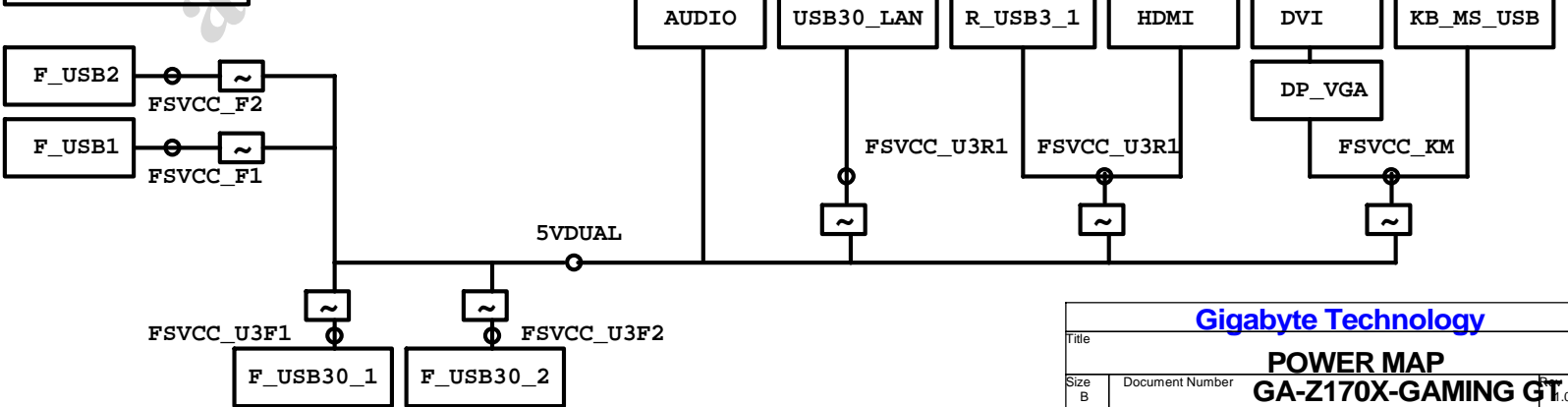
VCORE/VCCGT



POWER



FUSE POWER F/R



固態電容料號.請自行修改

日系黑色固態	Capture Value
11C02-C85600-01R	560u/FP/D/6.3V/68/C/8m
11C05-C82700-01R	270u/FP/D/16V/88/C/12m
11C05-C61000-01R	100u/OS/D/16V/66/C/30m
11C02-C51000-01R	100u/FP/D/6.3V/65/C/13m

日系一般固態	Capture Value
11C02-685600-01R	560u/FP/D/6.3V/68/8m
11C05-882700-01R	270u/FP/D/16V/88/12m
11C05-661000-03R	100u/OS/D/16V/66/30m
11C02-651000-02R	100u/OS/D/6.3V/66/30m

台系固態	Capture Value
11C02-661000-09R	100u/OS/D/6.3V/66/A/35m
11C05-691000-09R	100u/OS/D/16V/69/A/35m
11C05-8C2700-09R	270u/FP/D/16V/8C/A/10m
11C02-695600-09R	560u/FP/D/6.3V/69/A/11m

PWM料號

		料號	Capture Value	Footprint
PWM	ISL95856	10TA1-695856-01R		IC52QFN-6x6-G
PWM	ISL95858	10TA1-695858-01R		IC52QFN-6x6-G
PWM	IR35201	10TA1-635201-00R		IC56QFN-9VRS4339
PWM	IR3570	10TA1-603570-00R		IC40MLFP-ISL95835
PWM	RT8237C/D	10TA1-608237-01R		IC10DFN-NIS5132

REGULATOR

		料號	Capture Value	Footprint
	NCT3103S	10GL2-203103-01R	NCT3103S/SOP8/2A	IC8-EPSOIC

IRON CHOKE

	料號	Capture Value	SIZE	Footprint	
DIP	11LC5-M4500C-01R	0.5uH/40A/IMD109/M/D	10*10	CHOKE05U-40A-1PQ-3	閃電P
DIP	11LC5-M4500C-11R	0.5uH/40A/IMD109/M/NP/D	10*10	CHOKE05U-40A-1PQ-3	無閃電P
DIP	11LC5-M2500C-01R	0.5uH/20A/IMD0809/M/D	8*8	CHOKE1U-R50M-IF	


Skylake Iron Choke閃電P導入機種如下:
[1] Z170/H170 機種全部導入
[2] B150/H110Gaming機種導入, 其餘不導入

Ferrite

	料號	Capture Value	SIZE	Footprint
DIP	11LC5-F3500C-11R	0.5uH/32A/INCG109/FSI/D	10*10	CHOKE05U-40A-1PQ-3
DIP	11LC5-F2500C-11R	0.5uH/25A/INC0809/F/D	8*8	CHOKE1U-R50M-IF
SMD	10LC5-F4300C-01R	0.3uH/40A/SIUC/FR/S	10*7	CHOKE11X8MM-SMD

BEAD

	料號	Capture Value	SIZE	Footprint
DIP	10LFB-15470A-01R	47/4030/15A/S	4*3	BEADC8B-BPH_SMD



Title

RT8120_DDR4 POWER

Size Custom

Document Number

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Rev

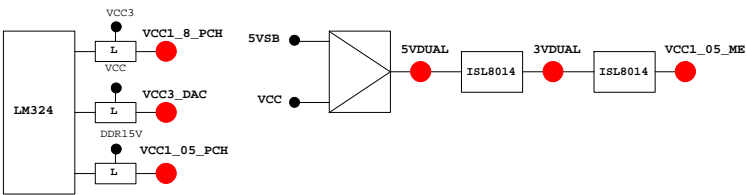
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PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

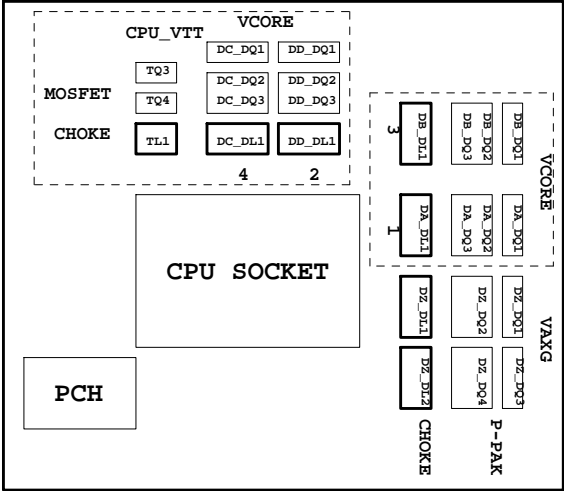
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCI_E_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSIO	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

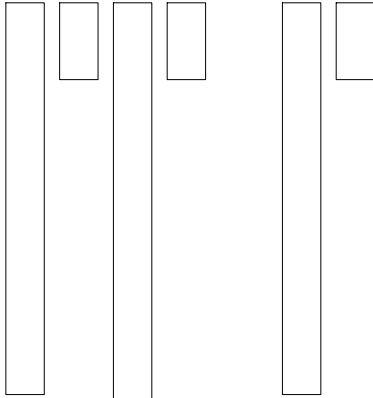
	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

REAR IO

RS_SYS

F_AUDIO

AUDIO



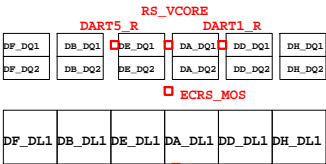
SIO

PCH

RS_PCH
ECRS_PCH

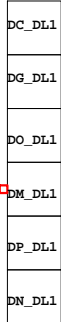
ECRS_SYS

SATA_EXPRESS



CPU

DDR_VS
DDR OUTPUT CAP



熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
RS_VCORE	DC_DQ4	N/A
RS_VCCGT	DM_DQ2	N/A
TTT1	DC_DQ2	N/A
TTT2	DN_DQ2	N/A
RS_PCH	PCH	N/A
RS_SYS	F_AUDIO	N/A

Thunderbolt™ 3 Intel® USB 3.1

